MVSR ENGINEERING COLLEGE
(An Autonomous Institution)

MASTER OF ENGINEERING

ACADEMIC REGULATIONS , SCHEME OF INSTRUCTION & SYLLABI (R-25)

ELECTRONICS & COMMUNICATION ENGINEERING
(I, II, III & IV Semesters)

ACADEMIC YEAR 2025-26

(Sponsored by Matrusri Education Society, Estd.1980

ISO 9001:2015

nirf 2020 Rank band 251-300

ACCREDITED BY NAAC NATIONAL ASSESSMENT AND ACCREDITATION COUNCIL

NBA Accredited Courses Civil,CSE,ECE, EEE,Mech & IT

R-25

Rules and Regulations for M.E. /M.Tech Programs

MVSR Engineering College

Nadergul, Hyderabad – 501510

(An Autonomous Institution)

Accredited by NAAC & NBA Program

2025

College Profile

MVSR Engineering College is established in 1981 and affiliated to Osmania University. Currently, the college has B.E programs in Civil, CSE, ECE, EEE, IT, Mechanical and Automobile Engineering, PG programs in Civil Engineering, CSE, ECE and Mechanical besides MBA. College is recognized by Osmania University as a Centre for pursuing research leading to the award of Ph.D. Degree in the Disciplines of CSE, ECE and Mechanical Engineering. In all about a 1000 students take admission every year. The college is one of the earliest of the private Engineering colleges in the state. Since inception, the college has ensured an excellent and exemplary academic standard which has helped the college to be one of the topmost and most sought after college in the state.

Vision:

- To Impart technical education of the highest standards, producing technically competent confident and socially responsible engineers.

Mission:

- To impart adequate fundamental knowledge, technical and soft skills to students.
- To make learning process exciting, stimulating and joyful.
- To create a climate conducive to excellent teaching - learning Process.
- To bring out creativity in students.
- To contribute to advancement of engineering & technology.
- To make positive contribution to meet societal needs.

MVSR Engineering College

Hyderabad

Quality Policy

To provide quality education in engineering

through continual upgradation of

Teaching - learning process,

Human resources and

Infrastructure

so as to produce competent and committed professionals.

Date: 01.06.2010

Place: Hyderabad

PRINCIPAL

Rules and Regulations

M.E. /M.Tech. Programs (Full-Time)

(Applicable to the students admitted from the Academic Year 2025-2026 onwards)

1. INTRODUCTION:

1.1 Provision of these rules and regulations shall come into force with effect from the academic year 2025-2026 and shall be applicable to all the M.E / M.Tech. courses offered by the Institute

1.2 All the rules and regulations, herein after specified shall be read as a whole for the purpose of interpretation.

2. GENERAL:

2.1 This document gives the general regulations applicable to all M.E. /M.Tech programs. Specific requirements for a particular M.E / M.Tech program are specified in regulations for that program.

2.2 Any condition arising in the PG program and not covered in this manual shall be referred to the PG committee, which may refer it to the academic committee / Council of the institute.

3. M.E /M.TECH PROGRAMS:

The M.E. / M.Tech programs are offered in the following specializations by the respective departments of the Institute.

Department	**Program**	**Course/ Specialization (s)**	**Minimum eligibility criteria**
Civil Engineering	M.E	Structural Engineering	B.E / B.Tech in Civil Engineering
Computer Science and Engineering	M.Tech	Computer Science and Engineering	B.E./B.Tech in CSE / IT and Allied Branches
Electronics and Communication Engineering	M.E	Embedded systems and VLSI Design	B.E/ B.Tech in Electronics and Communication Engineering
Mechanical Engineering	M.E.	CAD/ CAM	B.E. / B.Tech in Mechanical Engineering

3.1 ELIGIBILITY FOR ADMISSION*

An applicant for admission into the M.E. / M.Tech. Program shall have one of the following qualifications:

3.1.1 A Bachelor's degree in Engineering/Technology as mentioned against each specialization in the table 1 above, which is equivalent to the Bachelor's degree in Engineering / Technology of Osmania University.

3.1.2 AMIE Degree or similar qualification recognized by the UPSC as equivalent to B.E / B.Tech.

3.1.3 The candidates will be admitted strictly in accordance with the merit secured at the Entrance Examination conducted by the Government of Telangana, keeping in view of the rules in force regarding the reservations of seats to various categories of candidates.

*** Subject to review from time to time as per the directives of competent authority.**

3.2 HOW TO APPLY

A candidate seeking admission into the M.E./M.Tech. Program shall apply in the prescribed form as per the notification issued by Convener, PGECET (on behalf of TSCHE) every academic year.

3.3 ADMISSION

a) Admissions to Category ‘A’ will be filled by the Convener, PGECET appointed by TSCHE after conducting the counseling for admission to PG programs.
b) Admissions to category ‘B’ will be filled by the institute as per the norms from time to time.

The following documents are to be submitted at the time of admission

1. X and XII Std. Marks statement
2. Mark Sheets of all semesters/ years wise / consolidated of the qualifying degree examination, up to pre-final/ final year as applicable if result awaited.
3. Qualifying Degree / Provisional Certificate (If degree completed)
4. Transfer/Migration/College Leaving Certificate obtained from the Institute last studied (If already received)
5. Valid GATE Score Card (If available)
6. Community Certificate (only for SC/ST categories).
7. Nativity Certificate (for Jammu & Kashmir, Ladakh and North Eastern States)

4. COURSE STRUCTURE

4.1 The duration of M.E. / M.Tech. (Full – Time) Programme is 4 semesters. The total period of study for the purpose of drawing the scholarship amount (if eligible) shall not exceed 24 months. Each semester shall have 16 weeks of instruction.

4.2 The total course for an M.E. / M.Tech degree program will typically consist of the following components:

a.	Program Core Courses
b.	Program Elective courses
c.	Mandatory courses
d.	Audit courses
e.	Open Electives
f.	Mini project
g.	Laboratory
h.	Internship
i.	Major Project

M.E./M.Tech. Four Semester Program Scheme of Instruction and Evaluation

S.No.	Course Name	Contact hours per week			Scheme of Examination		Credits
		L	T	P	CIE	SEE	
	SEMESTER-I						
1.	Core-I	3			30	70	3
2.	Core-II	3			30	70	3
3.	Programme Elective-I	3			30	70	3
4.	Programme Elective-II	3			30	70	3
5.	Research Methodology and IPR	3			30	70	3
6.	Audit Course-I	2	1		30	70	0
7.	Laboratory-I	0		3	50	-	1.5
8.	Laboratory-II/Seminar-I	0		3	50	-	1.5
	TOTAL	**17**	**1**	**6**	**280**	**420**	**18**
	SEMESTER-II						
1.	Core-III	3			30	70	3
2.	Core-IV	3			30	70	3
3.	Programme Elective-III	3			30	70	3
4.	Programme Elective-IV	3			30	70	3
5.	Audit Course-II	2	1		30	70	0
6.	Mini Project with seminar			6	50		3
7.	Laboratory-III			3	50	-	1.5
8.	Laboratory-IV/Seminar-II			3	50	-	1.5
	TOTAL	**14**	**1**	**12**	**300**	**350**	**18**
	SEMESTER-III						
1.	Programme Elective-V	3			30	70	3
2.	Open Elective	3			30	70	3
3.	Major Project-I			20	100		10
	TOTAL	**6**		**20**	**160**	**140**	**16**
	SEMESTER-IV						
1.	Major Project-II			32		200	16
	GRAND TOTAL						**68**

CIE: Continuous Internal Evaluation SEE: Semester End Examination

Audit Courses – I& II	**Open Electives**
1.English for Research Paper Writing	1.Business Analysis
2.Disaster Management	2.Industrial Safety
3.Sanskrit for Technical Knowledge	3. Operation Research
4.Value Education	4.Cost Management of Engineering Projects
5.Constitution of India	5. Composite Materials
6.Pedagogy Studies	6. Waste to Energy
7.Stress Management by Yoga	
8.Personality Development through Life Enlightenment Skills	

5. PROGRAM FEE AND SCHOLARSHIP

5.1 Course fee will be informed at the time of admission. Each student shall pay the course fee and other fees as specified at the beginning of the academic year.

5.2 Eligible students joining with GATE rank will be given scholarship as per the norms. (See appendix III)

6. PROGRAM REQUIREMENTS

6.1 The degree of M.E./M.Tech. will be conferred on a candidate who has (a) pursued a regular course of study of not less than three semesters of course work as prescribed hereunder and has passed all examinations in the subjects as prescribed in the Scheme of Examination, and (b) submitted and successfully defended his/her Major Project at the end of the fourth semesters (Regular programme) as prescribed in the Scheme of Instruction and Evaluation.

6.2 A regular course of study for eligibility to appear in any subject, for which an examination will be conducted at the end of the semester shall mean putting in an attendance of not less than 75% in each of the subject registered during that semester.

6.3 However, in special cases and for sufficient causes shown, the competent authority may condone the deficiency of not exceeding 10% attendance for ill-health when an application is made for such a condonation supported by a medical certificate issued by an authorized medical officer and approved by the Institute. Absence not exceeding two weeks, for activities like N.S.S., Inter University Competitions and debates will be condoned if the candidate is sponsored by the institute for such activities.

6.4 If a candidate fails to secure the minimum of 65% attendance required in any subject, then he/she shall not be eligible to appear for the Semester End Examination at the end of the semester in the subject. He/she shall be required to pursue a regular course of study in the subject again before appearing for the Semester End Examination (SEE) in that subject.

6.5 If a candidate fails to maintain a minimum of 40% attendance in at least three of the Theory subjects registered independently (excluding Seminar and Laboratory courses) in the first semester following the admission, he/she shall forfeit his/her seat in the course and the admission automatically stands cancelled.

6.6 The course requirements will be as per AICTE Model Curriculum for PG courses in Engineering / Technology, January2018.

6.7 A student, on being admitted to the M.E / M.Tech. Programme will be assigned to a faculty Adviser / PG Coordinator. With the approval of the Faculty Adviser / PG Coordinator, the students shall draw up a study plan to satisfy all the requirements, keeping in view the area of specialization and then register for the courses.

6.8 A student shall not be allowed to register for more than two subjects along with the Major Project-II.

6.9 The registration process should be completed within one week from the date of admission for the I-semester and within one week from the date of commencement of classes for subsequent semesters. For the benefit of those who are unsuccessful in the main examination or for those who wish to reappear in a subject(s), a make – up examination will be conducted. A candidate must register for the main examination at the end of the semester. Failure to register for the main examination makes the candidate ineligible to register for the make-up examination.

6.10 In the event, the make-up examination results are not declared before commencement of new semester, the candidates may be provisionally permitted to register for the subject(s) / Major Project-I and continuation depends on the declared result.

6.11 A student is permitted for registration to Semester-III courses, if there are not more than three subjects as backlog from the previous semesters (Backlog for this purpose shall mean Theory courses/ Lab courses / Seminar). Moreover, the student is permitted for registration to Major Project-I, if he/she has completed the requirements of Mini Project. However, if this criteria is not satisfied in case of any student, he/she will be permitted for registration to Major Project-I in the subsequent even semester and for Major Project-II in the next odd Semester. A student without any backlogs will only be permitted to submit the Major Project. Major Project can be carried out at any recognized Institution/ R&D Organization with the approval of the Head of the Department and Head of the Organization.

6.12 In the first fortnight of the third semester of Full-Time Programme a student shall seek a faculty member of the college who will be willing to be his/her supervisor for the Major Project and register for it, failing which, the Head of the Department shall assign Supervisor. The student may, in addition, can also have an External Supervisor from the organization to which he / she is attached as a Co-supervisor with the approval of Head of the Department concerned.

6.13 A student shall submit five copies of the Major Project prepared in the standard prescribed format and approved by his / her supervisor on or before the date indicated in the almanac. The format specifications are given in Appendix. Detailed Guidelines on documentation of Major Project work will be issued separately.

6.14 For such of those candidates who have not completed the course to an extent of maximum of 2 subjects and/or the Major Project within the stipulated period, an additional period of one year in continuation may be given to complete the same by the competent authority on application duly recommended by the concerned Head of Department.

6.15 The maximum duration for completing all the requirements for obtaining the M.E./M.Tech Programme shall be N+2 (Where '**N**' stand for the normal or minimum duration prescribed for completion of the programme), which is four years from the date of admission.

7. EXAMINATION

7.1 All examinations shall be held by the Institute at such place and on such dates as may be notified.

7.2 Applications for permission to appear in SEE shall be made only through registration process on payment of the prescribed examination fee.

7.3 When a candidate's application is found in order and he/she is found eligible to appear in the Semester End Examination (SEE), the Examination branch, shall furnish him/her with a Hall Ticket for the Semester End Examination (SEE) and this Hall ticket shall have to be produced by the candidate before he/she is admitted into the examination hall.

7.4 A candidate is not entitled to claim refund of the whole or part of the examination fee nor for the reservation of the same for a subsequent examination (s) if he / she fails to present himself / herself for the Semester End Examination for any reason.

7.5 A student shall appear for the Semester End Examination at the end of each semester only in the subjects registered at the beginning of the semester.

7.6 A candidate will be permitted to apply for revaluation / recounting in any of the subjects appeared by paying the prescribed fee within five working days from the date of declaration of results.

7.7 A candidate will be permitted to appear for the make-up examination, which shall be conducted within one and half month from the declaration of the results of the main examination, in the subject(s) failed in the main examination. A candidate shall apply for the make-up examination in the specified format by paying the prescribed fee as per the notification issued by the examination branch. Without appearing in main examination, a candidate foregoes his/her chance to appear in make-up examination.

7.8 A candidate who is unsuccessful at both the main and make-up examination or has not appeared at these Examinations in [subject(s)] shall register for the subject (s) again and pass these core / elective course (s) as the case may be, irrespective of whether the syllabus remained same or revised. Further, the candidate who had undergone a regular course of study and secured a minimum of 75% attendance for eligibility to appear at the Semester End Examination can register for that course and appear for the SEE directly. The Continuous Internal Evaluation (CIE) marks earned earlier can be improved if the candidate wishes by appearing in the CIE. If the subject in which the candidate has failed is an elective, a new elective may be chosen if required. If a core course (subject) has been dropped in the curriculum, then the core course (subject) to be taken in place of the core course in which the candidate has failed will be specified by the Faculty Adviser / Course Coordinator in consultation with the Head of the department.

7.9 The distribution of Marks/Grades for the Continuous Internal Evaluation (CIE) and the Semester End Examination (SEE) areas detailed in the Scheme of instruction and Evaluation in table 2.

7.10 The SEE question paper will contain two parts, Part-A and Part-B. Part- A is for 10 Marks consisting 5 questions one from each unit, student should attempt all questions and each question carries 02 Marks. Part-B carries 50 marks with five questions (each Question carries 10 marks) covering all the five units with internal choice. Questions in part-B may have subdivision.

In theory subject, a candidate shall score i) 40% marks in Semester End Exam and ii) 40% of marks in Continuous Internal Evaluation and Semester End Exam (CIE+SEE) together, in a particular Course, to be declared as 'PASS' in that Course.

In Practical course, a candidate shall score i) 50% marks in Semester End Exam and ii) 50% of marks in Continuous Internal Evaluation and Semester End Exam (CIE+SEE) together, in a particular subject, to be declared as 'PASS' in that subject.

7.11 In CIE, out of **40 marks, 30 marks** are to be awarded on the basis of 2 class tests (taking average of both tests). Performance of both the tests will be taken into account. Remaining 10 marks are to be awarded based on assignments / seminars / quizzes etc.

7.12 A minimum of 50% of students or 4 (four) number of students (whichever is the least) must have registered to offer a Program Elective or Open Elective.

7.13 Laboratory Courses and Seminar listed in the **Scheme of Instructions and Evaluation** are Departmental requirements only. However, the candidate has to complete the same by securing Minimum qualifying marks.

7.14 For Laboratory courses, out of 50 marks, 30 marks are to be awarded by the faculty concerned. The remaining 20 marks are to be awarded based on the performance of the individual student in Viva-Voce / Quiz etc.

7.15 Each student is allotted a Mentor/Faculty member to complete Mini Project. Seminar has to be presented on completion of the Mini Project. Out of 50 marks, 30 marks are to be awarded by the mentor and 10 marks are to be awarded by each of the two examiners.

7.16 During Semester III of Regular Programme, student is expected to present Seminar on Major Project topic covering progress of problem of Major Project topic.

7.17 The evaluation of Major Project-I consists of 100 marks, of which 50 marks are to be awarded by supervisor and 50 marks to be awarded by internal Viva-Voce committee comprising Chairperson/Head of the Department and two Internal Faculty Members or one internal faculty and one external examiner as examiners. Each internal examiner willaward20marks and Chairperson will award 10marks.

7.18 During Semester IV of regular programme, the candidate will continue his/her Major Project work on the same topic and complete it by the end of semester. The candidate should examine his/her Major Project work checked for plagiarism by the software provided by the institute. The candidate can submit his/her Major Project, when the similarity index is less than 30%.

7.19 A student who has successfully completed all the programme requirements, is eligible to submit the Major Project.

7.20 Students who fail to submit their Major Project and complete the examination formalities at the end of fourth semester (as per the almanac notified) need to re-register for their Major Project work in the following semester (in no case later than the N+2 from the date of admission), where '**N**' stands for the normal or minimum duration prescribed for completion of the programme. They will have to pay the prescribed fee for re-registration of Major Project work every semester till the completion of their Major Project work.

8. MAJOR PROJECT WORK AND EVALUATION PROCESS:

Every candidate shall be required to submit thesis or Major Project after selecting a topic approved by the Project Review Committee.

8.1 Project Review Committee (PRC) shall be constituted by the Principal, Chairman BOS which consists of HOD as chair, PG Coordinator as Supervisor and Senior Faculty members of the Department.

1. Registration of Project work: A candidate is permitted to register for the project work in Third Semester.

2. The candidate has to submit his project proposal in consultation with his projects supervisor, the title, objective and plan of action of his/her project work to the PRC for its approval. Only after obtaining the approval of PRC the student can initiate the Project work.

3. If a candidate wishes to change his supervisor or topic of the project be can do so with approval of PRC. However, the PRC shall examine whether the change of topic/ supervisor leads to a major change of his initial plans of project proposal, If so, his date of registration for the project work start from the date of change of supervisor or topic as the case may be.

4. At the end of the III Semester, the project work progress is to be evaluated for 100 marks by the PRC Committee.

5. A candidate can submit project thesis only after successful completion of all theory and practical courses without any active backlogs and approval of PRC not earlier then 40 weeks from the date of registration of project work. For the approval of PRC the candidate shall submit the draft copy of the thesis to the Head of the Department and shall make an oral presentation before the PRC.

6. Three copies of the Project thesis certified by the supervisor shall be submitted to the concerned Head of the Department.

7. The external examiner for the final Viva-Voce examination shall be selected by the Dean (Examinations) along with Dean (Academics) of MVSREC and for this the Head of the concerned Department shall submit a panel of 5 examiners, who are eminent in that field with the help of the concerned guide.

8. Final Viva-Voce examination shall be conducted by a Board consisting of the External Examiner, Head of the Department, Supervisor and Project Coordinator.

8.2 The candidate who has passed all the courses and Departmental requirements has to present the Major Project-II to the internal Viva-Voce Committee. The Major Project shall be scrutinized and evaluated by the Viva-Voce committee consisting of the Head of the Department, Internal Examiners and Supervisor of the candidate. The Head of the department is the Chairperson of the Viva-Voce Committee and Department PG coordinator/ project coordinator is the Convener. The Viva-Voce will be conducted as per the Almanac and will normally be twice in an academic year.

8.3 The Viva-Voce committee will give a comprehensive report indicating the adequacy or otherwise of the Major Project-II, If candidate's Major Project -II work is found inadequate by the Viva-Voce committee, he/she has to appear once again for the Viva – Voce examination. The candidate will have to revise the Major Project-II as per recommendations of the Viva-Voce committee. The Department shall arrange for the conduct of pre-submission Viva-Voce and submit the final copy within two weeks to the Examination branch for conduct of Viva-Voce in consultation with the concerned Head of the department.

8.4 Within four weeks from the date of submission to the Exam branch, the external Viva-Voce examination shall be conducted. The external Viva-Voce Committee consists of the Head of the Department, External Examiner and Supervisor of the candidate. The evaluation of Major Project-II for maximum of 200 marks will be done as per the guidelines given below.

1) 70 Marks are allocated for quality of Major Project work covering
   I. Literature review
   II. Innovation/Originality
   III. Research Methodology adopted and
   IV. Relevance/Practical applications by supervisor.

2) 70 Marks are provided for Report writing/ Documentation

3) 30 Marks are allocated for quality and clarity of presentation of Major Project work.

4) 30 Marks are provided for candidate's performance in terms of his/her ability to defend the work, his/her ability to answer the queries raised during Viva-Voce examination and overall subject knowledge.

Total = (a+b+c+d= 200 Marks)

8.5 The formats for pre submission Viva-Voce and final Viva are given in Annexure I & II respectively.

9. AWARD OF DEGREE

A candidate shall be deemed to have fully passed in the subjects he/she has registered during the semester, if he/she secures not less than the minimum marks prescribed below:

Minimum Qualifying Marks

Course particulars	Exam	Minimum Marks / Grade
(i) Each Theory Course	(CIE+SEE)	**40% in SEE**
(ii) Each Laboratory Course (iii) Each Seminar (iv) Major Project-I (v) Major Project-II	(CIE) (CIE) (CIE) (SEE)	50%-‘D’ Grade

10. GRADING SYSTEM

Grades are awarded based on the combined marks secured in the Semester End Examination (SEE) (Maximum 70%) and Continuous Internal Evaluation (CIE) (Maximum 30%) as per the criteria stated in the following Table:

Academic Performance	Letter Grade	Grade Points
90%= Marks≤100%	A+	10
80% = Marks<90%	A	9
70%= Marks<80%	B	8
60% = Marks<70%	C	7
50%= Marks<60%	D	6
0%≤Marks <50%	F	0

i) The Memorandum of marks of a candidate will reflect the grade secured by him / her as per the grading criteria described in the table above.
ii) There is no minimum marks criteria for the Continuous Internal Evaluation (CIE) for theory subject(s).
iii) A minimum Cumulative Grade Point Average (CGPA) of 5 is required for the award of Degree. The consolidated memorandum of marks will reflect the credits / grade scored in each subject.

Semester Grade Point Average (SGPA) & Cumulative Grade Point Average (CGPA) Calculation:

(a) A student is said to have earned credits if he / she secures letter grade ‘D’ and above

(b) $$\text{SGPA} = \frac{\sum [\text{Letter Grade Point} * \text{Credits}]}{\sum \text{Credits}}$$

SGPA is calculated up to second decimal point
SGPA is calculated only when all subjects in that semester are Cleared/ Passed

(c) $$\text{CGPA} = \frac{\sum [(\text{SGPA}) * (\text{Total Credits})]}{\sum (\text{Total Credits})}$$

CGPA at a given point of Semester is calculated up to second decimal point CGPA is calculated only when total credits earned are equal to total credits up to a Semester in which the candidate has last appeared for Semester End Examination

(d) Memorandum of Marks should indicate total number of credits and total number of credits earned up to a point of Semester

10.1. In case of hearing impaired, orthopedically handicapped and visually challenged candidates, 10% reduction in pass marks in each subject is admissible as per G.O. Ms.No.150, dated 31-08-2006.

10.2. A candidate desiring to have recounting / revaluation can apply for it as per the institute norms and notification of Exam branch.

10.3. A candidate can also obtain a photocopy of the corrected answer book of the theory subjects SEE only on payment of Rs.1000/- (Rupees One thousand only) for each subject as per the notification of Exam branch.

10.4. In order to qualify for a PG degree of the institute, a student

1. Must have completed all the credit requirements for the degree as prescribed from time to time
2. Must have obtained a CGPA of at least 5.00 at the end of the semester in which the student completes all the requirements (including Major Project) for the degree

11. AWARD OF GOLD MEDAL

A student securing highest CGPA in **single attempt** is eligible for award of Gold Medal.

12. TRANSITORY REGULATIONS

1. Whenever the schemes of Instruction and /or syllabi are changed for a course, candidates shall satisfy the unfulfilled requirements of passing the number of core subjects and electives choosing equivalent subject/s from the revised schemes, with the approval of the competent authority.

2. Whenever a course or scheme of instruction has changed in a particular semester/year, two more examinations immediately following thereafter shall be conducted according to the old syllabus/regulations provided the content in the course has changed more than 40%.

3. Candidates not appearing at the examinations or failing in them shall register/appear for the examination subsequently according to the changed syllabus / regulations.

MALPRACTICE AND AWARD OF PUNISHMENT

Regulations under Ordinance no. vii

Conduct of Examinations Part – V

Schedule on the Nature of Malpractice and Award of Punishment

"Examination" in this context refers to all the papers taken by the candidate on the same hall-ticket.

S.No.	Malpractice	Award of Maximum Punishment
1.	Possession of the prohibited (written or printed) papers, books, notes during the examination period but which were not used.	Shall be debarred from appearing at the subsequent papers of the examination apart from cancelling the result of the examination in which he/she had indulged in malpractice.
2.	Matter relevant to the examination being written on any part of the body or on the clothes worn, or in the instruments, wrappings, etc.	-do-
3.	Attempting to take help from any prohibited papers, notes, written or printed matter, writings on the walls, furniture and attempting to take help from or giving help to other regarding answer to any question or questions of the examination paper.	-do-
4.	Taking help from or consulting of prohibited written or printed material; consulting and/or taking help from or helping other examinee during the examination period inside the examination hall or outside it; with or without their consent, or helping other candidate to receive help from anyone else.	-do-
5.	An examinee who attempts to disclose his/her identity to the paper valuer by writing his/her roll number at a place other than the place prescribed for it, or by writing his/her name or any coded message or an examinee who makes an appeal to the paper valuer in the answer book.	Cancelling the result of that paper
6.	Writing such as invocation of God's name in any form.	To be ignored
7.	Writing on the question paper or other papers; the answer to questions, rough work, etc., with no intention of passing it on to another examinee.	To be warned not to do so

8.	Using abusive and obscene language in the answer book.	Cancellation of the result of that paper
9.	Examinee allowing or destroying prohibited material found in his possession or acting in any other manner with a view to destroy evidence.	Cancellation of the result of all examinations taken or proposed to be taken during that session and prohibiting his/her admission to or continuation in any course for a period of one year.
10.	Refusing to obey instructions of the Chief Superintendent/Invigilator	Cancelling the result of that paper
11.	Smuggling an answer book /additional answer book/ matter into or out of the examination hall.	Cancellation of the result of all examinations taken or proposed to be taken during that session and prohibiting his/her admission to or continuation in any course for a period of one year.
12.	Inserting in or removing from the answer book/additional answer book of any sheet.	-do-
13.	Substituting wholly or partly an answer book/additional answer book.	-do-
14.	Impersonation even at a single examination.	To be dealt with as per law
15.	Cases of examinees when conspiring to interchange in Roll Numbers.	Cancellation of the result of all examinations taken or proposed to be taken during that session and prohibiting their admission to any course for a period of one year.
16.	Creation of disturbance or otherwise misbehaving in and around the examination hall during or before the examination.	Cancelling the results of all examinations taken or proposed to be taken during that session and prohibiting admission into or continuation in any course of study for a period of two years.
17.	Guilty of assaulting/abusing intimidating any person connected with the examination work any time before, during or after the examination	Cancelling the result of all examinations taken or proposed to be taken during that session and the next session and prohibiting admission into or continuation in any course for a period of two years.
18.	Punishments for malpractices not defined here would be recommended on the merits of the individual cases by the malpractices committee.	

APPENDIX I
Format of M.E./M.Tech. Major Project

Department of CSE / MECH / CIVIL / ECE

MVSR Engineering College

CERTIFICATE

This is to certify that the Major Project work entitled <Title of the Project Work> submitted by < Mr. / Ms. Name of the student (Roll No.) >, a student of Department of < Name of the Department >, < Name of the College > in partial fulfillment of the requirements for the award of the degree of master of <Engineering/Technology> with <Name of the Specialization> as specialization is a record of the bonafide work carried out by < him / her > during the academic year <Academic year >.

Date of submission of thesis

Signature of the Supervisor

Signature of Head of the Dept.

Seal

DECLARATION

I declare that the work reported in the Major Project entitled < Title of M.E. / M. Tech. Thesis> is a record of the work done by me in the Department of <Name of the Department, Place/Organization>. No part of the thesis is copied from books / journals / internet and wherever referred, the same has been duly acknowledged in the text. The reported data are based on the Major Project work done entirely by me and not copied from any other source.

Signature of the Student

Plagiarism Certificate

This is to certify that the thesis entitled '**Title of the Major Project'** submitted by **Name of the candidate**, towards partial fulfillment of the requirements for the award of the **Master of Engineering/Technology** degree in Engineering with specialization in **Specialization Name** was analyzed for Plagiarism. The Similarity Index was found to be ------% which is less than 30% as per the Faculty of Engineering norms.

Originality Report			
17%	**12%**	**10%**	**8%**
Similar Index	**Internet Sources**	**Publications**	**Student Papers**

(Signature of the Student) **(Signature of the Supervisor)**

(Signature of the Principal/Coordinator, Anti-Plagiarism Software)

Station: Hyderabad
Date:

Appendix II

Guidelines for preparing M.E./M.Tech. Major Project

The Thesis must be presented on A-4 paper approximately 11 inches/9 inches or 27.9 cm/ 22cm and duly hard bound.

I. General:

1. The title of the thesis should be concise and clearly convey the work presented.
2. Lists of figures, tables, variables, symbols, acronyms etc., should be included, before the start of the first chapter.
3. The abstract should not be more than 500 words.
4. A declaration stating the originality of work / results should be appended.
5. Any work which amounts to plagiarism should be totally avoided.
6. The entire thesis should be free from grammatical and spelling mistakes.
7. The total number of pages of the thesis should not normally exceed 250.
8. Any downloaded matter of tables or equations, if used, should be rewritten, and the source mentioned.
9. The first Chapter should clearly reflect the importance and objectives of the thesis.
10. A brief literature review may be included in the first or second chapter.
11. The organization of the thesis may be mentioned in the first chapter.
12. The pages should be numbered starting from the first page of the first chapter.
13. The pages before the first chapter should be numbered in small Roman numerals.
14. The headings and sub-headings should be properly numbered chapter wise.
15. Extension work may be indicated in the conclusion.
16. Uniform font and size should be followed for the titles of all chapters.
17. Uniform Indent should be followed throughout the text of the thesis.
18. Similarly uniformly should be maintained for all headings and sub headings.
19. Subscripts and superscripts should be adopted properly.

II. Formatting

1. The text should be presented at one and a half spacing.
2. The font size of the main text should be uniformly12 points throughout the thesis.
3. Left justification or left and right justification can be used for main text.
4. The left margin should be 30 -40 mm and the right. Top and bottom margins should be 25to 30 mm.
5. The final Major Project copies should be hard bound in PURPLE colour rexin. The cover page should be gold embossed. On the spine of the Major Project the full name of the candidate and the year of submission should be gold embossed.

III. References

1. The references should be numbered from the first chapter to the last chapter in ascending order and the corresponding number should be shown in square brackets wherever required.
2. The reference should be listed with details after the last chapter.
3. All the references listed should be referred in the main text.
4. The references could be technical papers of Journals, conferences, symposia, workshops and seminars, technical reports, manuals, textbooks and software.
5. The important contents of referred materials should be in the following order: Name (s) of the author (s), Title of the paper, publication title, year of publication, Vol, No., pp.

IV. Appendices

1. Important programs, derivations, data and any other useful material may be shown in the appendices with proper numbering.
2. The appendices should be numbered in capital Roman numbers or capital letters from the first chapter to the last chapter in ascending order. (e.g. Appendix1 or Appendix A)
3. The appendices should be shown with details after the last chapter.
4. All the appendices should be referred in the main text.

V. Equations

1. All the equations used in the thesis should be properly numbered chapter wise (eg.Eq,3.1or)
2. The equations shown should be clearly referred and identified as Eq. or eq. followed by equation number.
3. Repetition of equations should be avoided. If needed, it may be referred by its number.
4. Equations should never be mixed up with main text. It should be shown as separate object and ‘Equation Editor’ can be used.

VI. Tables

1. The tables shown in the thesis should be clearly referred and explained and they should be numbered properly.
2. At the top of the table, it should be identified as table, followed by table number (ex.Table3.1)
3. The caption of the table should be written clearly, precisely and briefly at the same position.
4. A spacing of at least 3 points should be taken for the first line of each cell.
5. Table size should not cross the limits of the set page margins.
6. The font size should be less than or equal to the font size of main text.

VII. Figures

1. The figures shown in the thesis should be clearly referred and explained. They should be numbered properly chapter wise.
2. At the bottom of the figure, it should be identified as fig. or figures, followed by figure number (ex. Fig3.1 orfigure3.1).
3. The caption of the figure should be written clearly, precisely and briefly at the same position.
4. All the graphs and flowcharts should be identified and presented the same way as figures.
5. All the figures and graphs should be drawn clearly, so that variables, units, markings and details are dissembled.
6. All the drawings, textboxes, images and details related to a particular figure should be grouped together.
7. The font size used should be less than or equal to the font size of main text.
8. The figure size should not exceed the set page margins.

Appendix III

AICTE - Post Graduate (PG) Scholarship

1.0 Objectives of the Scheme:

1.1. AICTE: In order to ensure development of technical education in India awards Post Graduate Scholarship of Rs.12,400/- per month to full-time GATE/GPAT qualified students admitted to AICTE approved post graduate programs in AICTE approved Institutions/ University Departments as per AICTE approved intake.

1.2. Amount of Scholarship: The Scholarship under the scheme is Rs.12,400/- per month per student.

1.3. Duration: a) The Scholarship is tenable for 24 months or for the duration of the course i.e. from the date of commencement of classes till the date of completion of the classes whichever is lower and is not extendable under any circumstances. b) Students of final years of dual degree integrated programmes would also be entitled to PG Scholarship from the 9th semester onwards in case they get a CGPA score of 8 or above (on a scale of 10) i.e. only for one year in final year.

1.4. Eligibility for Scholarship: Post Graduate Scholarship is entitled only to those students

i. Having a valid GATE/ GPAT score at the time of admission.

ii. Must be admitted as a full-time scholar.

iii. Students of final years of dual degree integrated programmes would also be entitled to PG Scholarship from the 9th semester onwards in case they get a CGPA score of 8 or above (on a scale of 10) i.e. only for one year in final year.

iv. Admitted in AICTE approved Institutions / University Departments & AICTE approved programs viz. Master of Engineering, Master of Technology, Master of Architecture and Master of Pharmacy.

v. Number of PG Scholarship is limited to the AICTE approved intake in the programme in that year. However in addition to the approved intake, AICTE will provide PG scholarship to the additional 10% candidates over and above the approved intake of that course from EWS category, if the university/ institute has admitted students from Economically Weaker Sections (EWSs) as per MHRD OM F.No.12-4/2019-U1 dated 17th January 2019.

1.5 Other Entitlements: Students are eligible for following leaves:

- Casual leave: 15 days in an academic year
- Medical leave: Maximum of one month (30 days) in an academic year
- Maternity leave : Candidates are eligible for maternity/ Paternity leave as per Govt. of India norms issued from time to time at full rates of scholarship etc. once during the tenure of their award. However maximum duration of scholarship will not be extended in any circumstances.

Note: All kinds of leaves should be approved at the level of the University/College/Institute. Prior approval of the University/Institution/College is mandatory for all types of leaves.

1.6 Terms and Conditions:

I. In case any student/scholar receives any financial assistance from any other organization during the tenure of course, with due permission of the university/institute, the scholar will not be entitled for the scholarship for the duration in which he/ she is availing such financial assistance and it shall be resumed on discontinuance of such external financial assistance. Further the period for which the scholar has received external financial assistance shall be deducted from the maximum duration of the scholarship.

II. Foreign students, sponsored candidates and candidates admitted in PG programs through management quota are not eligible for the Scholarship.

III. It will be obligatory for every post-graduate student to undertake 8 to 10 hours (per week) of work related to teaching and research activities as assigned to him /her by the Institute. This could include tutorials, laboratory classes, development and maintenance of laboratories, assistance in research and development activities undertaken by faculty members, maintenance and operation of Computers and other central facilities, assistance in library, etc.

IV. The Scholarship will be granted to the student on a monthly basis subject to the satisfactory academic performance and adherence to University/Institute norms/rules and regulations as applicable time to time, certified by the Head of the Institute and obligatory work as per point no (iii) above.

V. PG Scholarship is not admissible to passed out students taking 2nd time admission on the basis of re-qualifying GATE/GPAT exam who have already availed the scholarship from AICTE or any other centrally funded institution like – IITs, NITs and IIITs etc. vi) The amount of PG Scholarship is subject to change as per the notification issued by Ministry of Human Resource Development (MHRD), New Delhi (now Ministry of Education) from time to time, with the approval of the Executive Committee of the Council.

VI. The student shall be required to give an undertaking to the effect that he/she would not leave the course midway. In case any student leaves the course in midway or failed/ drop out in subsequent year, he/she will be required to refund the total PG Scholarship drawn at the time of leaving the course. For those scholars who left the course midway on or after 1st October 2020, the scholarship shall be stopped.

VII. The Scholarship may be discontinued at any time for any kind of misconduct by the student, like involving in the act of ragging, misbehavior etc. on the recommendations of the Head of Institution (HOI).

VIII. Salary grant or any other grant e.g. Contingencies, Library, Books etc, will not be admissible to the Institute/College/ University implementing this scheme in compliance with the instructions of Govt. of India, Ministry of Human Resource Development, Dept. of Higher Education, Technical Section – I conveyed vide letter No. F. No. 9-2/2007-TS.I dated 22nd July, 2008.

IX. The mode and procedure of payment of Scholarship to the students shall be governed by the policy decision of the AICTE as may be notified from time to time on its web-portal or through advertisement in leading English/Hindi newspapers.

X. Any belated claim preferred after one year of the completion of the program shall not be entertained.

XI. The AICTE may impose any other conditions as deemed necessary from time to time and the decision of the AICTE shall be final and binding upon the recipients i.e. University/Institute/College/Student who are under the ambit of the AICTE for receipt of PG Scholarship.

XII. In case any student/scholar avails the break during the scholarship period on medical ground with due permission of the university/institute, the scholarship will be discontinued from the month of such break and shall be resumed on rejoining the program for the remaining period of scholarship.

Appendix IV

STUDENTS' CONDUCT AND DISCIPLINARY CODE

It is the responsibility and duty of each and every student of the Institute to become acquainted with "Students Conduct and Disciplinary Code". It is presumed that every student from the date of his/her admission to the Institute has knowledge of this code. All students are required to strictly adhere to this code as a condition of their admission to the Institute and these rules would be binding on and enforceable against them or any one among them.

Section 1: Responsibilities of the Students: It shall be the responsibility of the students

i. To behave and conduct themselves in the Institute campus, hostels and premises in a dignified and courteous manner and show due respect to the authorities, employees and elders.

ii. To follow decent and formal dressing manners. Students should avoid clothing depicting illegal drugs, alcohol, profane language, racial, sexual and vulgar captions etc.

iii. To access all educational opportunities and benefits available at the Institute and make good use of them to prosper academically and develop scientific temper.

iv. To respect the laws of the country, human rights and to conduct in a responsible and dignified manner at all times.

v. To report any violation of this Code to the functionaries under this Code.

Section 2: Behavior of the Students

1. Groupism of any kind that would distort the harmony is not permitted.

2. Students are expected to spend their free time in the Library. They shall not loiter along the verandas or crowd in front of the offices or the campus roads. Students should refrain from sitting on places such as parapets, stairs, footpaths etc.

3. Possession or consumption of narcotic drugs and other intoxicating substances are strictly prohibited in the campus and hostels.

4. Silence shall be maintained in the premises of the Institute.

5. Students are not permitted to use mobile phones in the class room, library, computer Centre, examination halls, etc.

6. Students shall refrain from all activities considered as ragging which is a criminal offence.

7. Students are prohibited from indulging in anti-institutional, anti-national, antisocial, communal, immoral or political expressions and activities within the campus and hostels.

8. Politically based students' and other organizations or outfits are not allowed in the campus. Students are strictly prohibited from organizing, attending or participating in any activity or agitation sponsored by politically based organizations.

9. Students shall not deface, disfigure, damage or destroy or cause any loss in any manner to all the public, private or Institute properties.

10. Without specific permission of the authorities, students shall not bring outsiders to the Institute or hostels.

11. No one shall bring, distribute or circulate unauthorized notices, pamphlets, leaflets etc., within the campus or hostels.

12. The possession, distribution or exhibition of any item by any means which is per se obscene is prohibited within the campus or on any property owned/ managed by the Institute.

13. No student shall collect money either by request or by coercion from others within the campus or hostels.

14. The Institute being a place of learning and an exclusive academic zone, nobody shall respond to any call for any form of strike, procession or agitation including slogan shouting, dharna, gherao, burning of effigy or indulge in anything which may harm the peaceful atmosphere of the Institution and shall eschew from violence in the campus and hostels and even outside.

15. Possession or usage of weapons, explosives or anything that causes injury/ damage to the life and limb or body of any human being or property is prohibited.

16. Use of motorized vehicles within the Institute premises is strictly prohibited.

17. Students shall only use the waste bins for dispensing waste materials within the campus including classrooms, hostels, offices, canteen and messes.

18. Any conduct which leads to lowering of the esteem of the Institute is prohibited.

19. Any tours / visits by group of students without prior approval from the Institute is strictly not permitted and will be viewed seriously.

Section 3: Disciplinary Sanctions:

1. Any student exhibiting prohibited behavior mentioned in this Code shall, depending upon the gravity of the misconduct or depending on its recurrence, be subjected to any of the following disciplinary sanctions.

2. Any student who is persistently insubordinate, who is repeatedly or willfully mischievous, who is guilty of fraud, in the opinion of the competent authority, is likely to have an unwholesome influence on his/ her fellow students, will be removed from the rolls.

I. Minor Sanctions

i. Warning or Reprimand: This is the least sanction envisaged in this Code. The student engaged in any prohibited behavior will be issued a warning letter.

ii. Tendering Apology: The student engaged in any prohibited behavior may be asked to tender an apology for his/her act and undertaking that he/she shall not indulge in such or any of the prohibited behavior in future.

II. Major Sanctions

i. Debarring from Examinations: A student/group of students may be debarred from writing all/any/some of the examinations, which forms part of the academic program for which he/she/they has/ have joined.

ii. Suspension: A student may be suspended from the Institute for violation of any of the provisions of this Code. The period of suspension and conditions, if any, shall be clearly indicated in the communication addressed to the student. The student shall lose his/her attendance for the suspended period.

iii. Restitution: Restitution implies reimbursement in terms of money and/or services to compensate for personal injury or loss, damage/disfiguration to property of the Institute or any property kept in the premises of the Institute in any manner. The students/group of students may be asked to compensate for the loss that has been caused to any person or property of the Institute or any property kept in the premises of the Institute due to the act of vandalism perpetrated by the students. The students/group of students shall also be liable to put in their service to restore any loss or damage caused to any property and thereby bringing it to its original form if it is possible.

iv. Forfeiture: Caution deposit of any student engaged in any prohibited behavior shall be forfeited.

v. Expulsion: This is the extreme form of disciplinary action and shall be resorted to only in cases where stringent action is warranted. Expulsion is the permanent dismissal of a student from the Institute. Such a student will not be eligible for readmission to any of the courses of this Institute.

Section 4: Functionaries under the Code

i) **Heads of the Departments/ Faculty Advisors/Chief Warden/ Wardens of Hostels:** As the persons in charge of the Departments, the respective functionaries of all Teaching Departments shall have the power and duty to take immediate action to curb any prohibitory behavior as envisaged under this code.

As these functionaries cannot single handedly manage all the issues, they can assign part of the work to the teachers and the teachers of all the departments have the responsibility to inform any incident of prohibited behavior to the Heads of the Departments so that any serious issue can be settled before the same goes out of control. The Head of the Departments shall have the power to impose minor sanctions envisaged under section 3(I) of this Code.

They can also recommend imposition of major sanctions as envisaged under Section 3(II) of this Code to the Director. The Head of the Departments/ Faculty Advisors while taking any action as envisaged in the code shall do so in an impartial manner and see to it that the sanction imposed/proposed is commensurate with the gravity of the prohibited behavior. Any lapse on the part of a teacher/ Warden to report any instance of violence and misconduct on the part of the students shall be reported to the Director by the respective Head of the Departments/Chief Warden.

The Wardens of Hostels shall be responsible for maintaining strict discipline and decorum in the hostel. He/she shall specifically see to it that the inmates of the hostel do not involve themselves in violation of any clause under Section 2 of this Code.

ii) **Deans:** Any authority of the Institute with delegated powers shall have the power to visit/inspect any premises, buildings or any property of the Institute when there is a genuine doubt that any act of prohibited behavior is taking place and can take any lawful actions to curb such behavior. The HODs/ Faculty Advisors/Chief Warden/ Wardens of Hostels shall report to the Dean (Students) any instances of prohibited behavior, who in turn shall bring it to the notice of the Director. The Dean (Students) shall forward the recommendations from the HODs/ Chief Warden to impose a major sanction under Section 3(II) of this Code to the Director after noting his observations. The Dean (Students) can also suo moto recommend action against any student/students indulging in prohibited behavior which is brought to his/ her notice.

iii) **Principal:** The Principal shall be the ultimate authority in imposing major sanctions as envisaged under Section 3(II) against the students for acts of prohibited behavior. The Principal can also entertain any appeal from any student/students aggrieved by the action of any authority of the Institute under or subordinate to the Principal and decide the case on merit.

Section 5: **Right to Appeal:**

The student/students aggrieved by the action of any authority of the Institute under or subordinate to the Principal can appeal to the Principal.

Section 6: Assistance from Law Enforcement Agencies:

The Deans/ HoD shall have the power and duty to call the Police immediately with the concurrence of the Principal when there is a threat of Law and Order situation in the Campus and also when there is a genuine apprehension that any incident of rioting, vandalism or any other act prohibited by law is likely to take place. The Deans/ HoDs/ Chief Warden shall in such a case give a detailed report to the Principal. The Principal/ Deans/ HoDs/ Chief Warden can also arrange for video recording of the entire situation and take requisite actions through police and other concerned. Authorities

Section 7: Grievance Redressal Committee

The Institute will also set up “Grievance Redressal Committee” where the students can air their grievances. The Committee shall consist of the Deans/ HoDs/ Chief Warden and also members of the Parent-Teacher Association. Till these committees are constituted, ad-hoc committees shall be formed by the Director.

Section 8: Undertaking by the Students

The students joining any academic program of the Institute will have to give an undertaking to the effect that he/she will comply with the provisions envisaged in this Code in letter and spirit and even if it is not given them as well, will be bound by the provisions of this Code.

Section 9: Opportunity for Hearing

No order other than the order suspending or warning a student shall be passed without giving an opportunity of hearing to the Student/ Students.

Section 10: Ultimate Authority

For all disciplinary matters related to students, the Principal shall be the ultimate authority as provided herein.

Section 11: Amendments to the Code

The administrative council of the Institute shall have the power to amend any of the provisions in this Code. The amendments shall be brought to the notice of the students and faculty of the Institute through notice put on the institute website, notice boards of the institute or through emails.

Scheme of Instruction & Examination

(with effect from the academic year 2025-2026)

M.E. I to IV Semester
of
Two Year Post Graduate Degree Programme
&
Syllabus of M.E. I to IV Semester
Specialization in
EMBEDDED SYSTEMS AND VLSI DESIGN

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

MVSR Engineering College

(Sponsored by Matrusri Education Society, Estd. 1980)

(Autonomous Institution)

Accredited by NBA & NAAC
Nadergul, Hyderabad - 501510

www.mvsrec.edu.in
2025

MVSR ENGINEERING COLLEGE

NADERGUL, HYDERABAD-501510

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An Autonomous Institution

Approved by AICTE & Affiliated to Osmania University,
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website: www.mvsrec.edu.in

SCHEME OF INSTRUCTION & EXAMINTATION-R25

M.E. (Electronics and Communication Engineering)
Specialization in **Embedded Systems and VLSI Design**

S.No.	Course Type / Code	Course Name	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
SEMESTER-I										
1.	Core	Programme Core–I	3	-	-	3	40	60	3	3
2.	Core	Programme Core–II	3	-	-	3	40	60	3	3
3.	Elective	Programme Elective–I	3	-	-	3	40	60	3	3
4.	Elective	Programme Elective–II	3	-	-	3	40	60	3	3
5.	Elective	Programme Elective–III	3	-	-	3	40	60	3	3
6.	MC	Mandatory Course	3	-	-	3	40	60	3	3
Practical/Laboratory Courses										
7.	Lab	Laboratory–I	-	-	2	2	25	50	-	1
8.	Lab	Laboratory–II	-	-	2	2	25	50	-	1
Total			**18**	**0**	**4**	**22**	**290**	**460**	**18**	**20**
SEMESTER-II										
1.	Core	Programme Core–III	3	-	-	3	40	60	3	3
2.	Core	Programme Core–IV	3	-	-	3	40	60	3	3
3.	Elective	Programme Elective– IV	3	-	-	3	40	60	3	3
4.	Elective	Programme Elective–V	3	-	-	3	40	60	3	3
5.	OE	Open Elective	3	-	-	3	40	60	3	3
Practical/Laboratory Courses										
6.	Lab	Laboratory–III	-	-	2	2	25	50	-	1
7.	Lab	Laboratory–IV	-	-	2	2	25	50	-	1
8.	Seminar	Seminar with Technical Writing	-	-	2	2	50	-	-	1
Total			**15**	**0**	**6**	**21**	**300**	**400**	**15**	**18**
SEMESTER-III										
1.	Audit	Audit Course	3	-	-	3	40	60	3	0
2.	Project	Major Project Phase–I	-	-	24	24	100	-	-	12
Total			**3**	**0**	**24**	**27**	**140**	**60**	**3**	**12**
SEMESTER-IV										
1.	Project	Major Project Phase–II (Dissertation)	-	-	36	36	-	200	-	18
		Total	**-**	**-**	**36**	**36**	**-**	**200**	-	**18**
									Grand Total	**68**

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M.E. (Electronics and Communication Engineering)
Specialization in **Embedded Systems and VLSI Design**

S.No.	Course Type / Code	Course Name	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
SEMESTER-I										
1.	Programme Core-I	Embedded System Design	3	-	-	3	40	60	3	3
2.	Programme Core-II	Analog VLSI Design	3	-	-	3	40	60	3	3
3.	Programme Elective-I	Hardware Software Co-Design Quantum Computing Advanced Computer Architecture	3	-	-	3	40	60	3	3
4.	Programme Elective-II	Low Power VLSI Design Semiconductor Device Modeling Microchip Fabrication Techniques	3	-	-	3	40	60	3	3
5.	Programme Elective-III	Machine Learning Mixed Signal Design Scripting Languages	3	-	-	3	40	60	3	3
6.	Mandatory Course	Research Methodology & IPR	3	-	-	3	40	60	3	3
Practical/Laboratory Courses										
7.	Lab-I	Embedded Systems Design Lab	-	-	2	2	25	50	-	1
8.	Lab-II	Analog VLSI Design Lab	-	-	2	2	25	50	-	1
Total			**18**	**0**	**4**	**22**	**290**	**460**	**18**	**20**
SEMESTER-II										
1.	Programme Core-III	Embedded Real Time Operating System	3	-	-	3	40	60	3	3
2.	Programme Core-IV	Digital IC Design	3	-	-	3	40	60	3	3
3.	Programme Elective-IV	System Verilog Multi gate MOSFET	3	-	-	3	40	60	3	3

		Technology VLSI Physical Design								
4.	Programme Elective-V	SOC Design DSP Architectures Embedded C	3	-	-	3	40	60	3	3
5.	Open Elective	Cost Management of Engineering Projects(CE) Business Analytics(CSE) Fundamentals of Embedded System Design (ECE) Waste to Energy(EEE) Industrial Safety (MED) Operational Research (MED) Fundamentals of Machine Learning (CSE) Real Time Operating System for Embedded Applications (ECE)	3	-	-	3	40	60	3	3
Practical/Laboratory Courses										
6.	Lab-III	Real Time Operating Systems Lab	-	-	2	2	25	50	-	1
7.	Lab-IV	Digital IC Design Lab	-	-	2	2	25	50	-	1
8.	Seminar	Seminar With Technical Writing	-	-	2	2	50	-	-	1
Total			**15**	**0**	**6**	**21**	**300**	**400**	**15**	**18**
SEMESTER-III										
1.	Audit Course	English for Academic and Research Writing Disaster Management Sanskrit for Technical Knowledge Value Education Constitution of India and Fundamental Rights Pedagogy Studies Stress Management by Yoga Personality Development through Life Enlightenment Skills	3	-	-	3	40	60	3	0
2.	Project	Major Project Phase–I	-	-	24	24	100	-	-	12
Total			**3**	**0**	**24**	**27**	**140**	**60**	**3**	**12**
SEMESTER-IV										
1.	Project	Major Project Phase–II (Dissertation)	-	-	36	36	-	200	-	18
		Total	**-**	**-**	**36**	**36**	**-**	**200**	**-**	**18**
Grand Total										**68**

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SCHEME OF INSTRUCTION & EXAMINTATION

M.E. (Electronics and Communication Engineering)
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Regulations-R25
SEMESTER-I

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			Credits
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	
1	P25PC001EC	Embedded System Design	3	-	-	3	40	60	3	3
2	P25PC002EC	Analog VLSI Design	3	-	-	3	40	60	3	3
3	Programme Elective	Programme Elective – I	3	-	-	3	40	60	3	3
4	Programme Elective	Programme Elective – II	3	-	-	3	40	60	3	3
5	Programme Elective	Programme Elective – III	3	-	-	3	40	60	3	3
6	P25MC001ME	Research Methodology & IPR	3	-	-	3	40	60	3	3
Practical/ Laboratory Courses										
7	P25PC801EC	Embedded Systems Design Lab	-	-	2	2	25	50	-	1
8	P25PC802EC	Analog VLSI Design Lab	-	-	2	2	25	50	-	1
Total			18	0	4	22	290	460	18	20

PC: Programme Core **PE:** Programme Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science **OE**: Open Elective

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination

Note:
1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. The Mandatory Course is offered in I-Semester

MVSR ENGINEERING COLLEGE

NADERGUL, HYDERABAD-501510

(Sponsored by Matrusri Education Society, Estd.1980)

An Autonomous Institution

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Accredited by NBA, NAAC
website: www.mvsrec.edu.in

SCHEME OF INSTRUCTION & EXAMINTATION

M.E. (Electronics and Communication Engineering)
Specialization in **Embedded Systems and VLSI Design**
Regulations- R25

SEMESTER-II

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	Credits
1	P25PC003EC	Embedded Real Time Operating System	3	-	-	3	40	60	3	3
2	P25PC004EC	Digital IC Design	3	-	-	3	40	60	3	3
3	Programme Elective	Programme Elective – IV	3	-	-	3	40	60	3	3
4	Programme Elective	Programme Elective – V	3	-	-	3	40	60	3	3
5	Open Elective	Open Elective	3	-	-	3	40	60	3	3
Practical/ Laboratory Courses										
6	P25PC803EC	Real Time Operating Systems Lab	-	-	2	2	25	50	-	1
7	P25PC804EC	Digital IC Design Lab	-	-	2	2	25	50	-	1
8	P25PC805EC	Seminar With Technical Writing	-	-	2	2	50	-	-	1
Total			15	0	6	21	300	400	15	18

PC: Programme Core **PE:** Programme Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science **OE**: Open Elective

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination

Note:
1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. The Mandatory Course is offered in I-Semester

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SCHEME OF INSTRUCTION & EXAMINTATION

M.E. (Electronics and Communication Engineering)
Specialization in **Embedded Systems and VLSI Design**
Regulations- R25

SEMESTER-III

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	Credits
1	Audit	Audit Course	3	-	-	3	40	60	3	0
2	P25PW801EC	Major Project Phase – I	-	-	24	24	100	-	-	12
Total			3	0	24	27	140	60	3	12

PC: Programme Core **PE:** Programme Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science **OE**: Open Elective

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination

Note:

1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the requirement of a particular laboratory.
3. The Mandatory Course is offered in I-Semester

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SCHEME OF INSTRUCTION & EXAMINTATION

M.E. (Electronics and Communication Engineering)
Specialization in **Embedded Systems and VLSI Design**
Regulations- R25

SEMESTER-IV

S. No.	Course Type/Code	Course Name	Scheme of Instruction				Scheme of Examination			
			L	T	P/D	Contact Hrs/Wk	CIE	SEE	Duration in Hrs	Credits
1	P25PW802EC	Major Project Phase- II (Dissertation)	-	-	36	36	-	200	-	18
Total			**-**	**-**	**36**	**36**	**-**	**200**	**-**	**18**

PC: Programme Core **PE:** Programme Elective **AD**: Audit Course
MC: Mandatory Course **HS**: Humanities and social science **OE**: Open Elective

L: Lecture **T**: Tutorial **P**: Practical **D**: Drawing
CIE: Continuous Internal Evaluation **SEE:** Semester End Examination

Note:

1. Each contact hour is a Clock Hour.
2. The practical class can be of two and half hour (clock hours) duration as per the Requirement of a particular laboratory.
3. The Mandatory Course is offered in I-Semester

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List of Subjects of Programme Core

S. No.	Course Code	Course Title
1	P25PC001EC	Embedded System Design
2	P25PC002EC	Analog VLSI Design
3	P25PC003EC	Embedded Real Time Operating Systems
4	P25PC004EC	Digital IC Design

List of subjects for Programme Elective I

S. No.	Course Code	Course Title
1	P25PE001EC	Hardware Software Co-Design
2	P25PE002EC	Quantum Computing
3	P25PE003EC	Advanced Computer Architecture

List of subjects for Programme Elective II

S. No.	Course Code	Course Title
1	P25PE004EC	Low Power VLSI Design
2	P25PE005EC	Semiconductor Device Modeling
3	P25PE006EC	Microchip Fabrication Techniques

List of subjects for Programme Elective III

S. No.	Course Code	Course Title
1	P25PE007EC	Machine Learning
2	P25PE008EC	Mixed Signal Design
4	P25PE009EC	Scripting Languages

List of subjects for Programme Elective IV

S.No.	Course Code	Course Title
1	P25PE010EC	System Verilog
2	P25PE011EC	Multi gate MOSFET Technology
4	P25PE012EC	VLSI Physical Design

List of subjects for Programme Elective V

S.No.	Course Code	Course Title
1	P25PE013EC	SOC Design
3	P25PE014EC	DSP Architectures
4	P25PE015EC	Embedded C

List of subjects for Open Elective

S.No.	Course Code	Course Title
1	P25OE001CE	Cost Management of Engineering Projects (CE)
2	P25OE002CS	Business Analytics(CSE)
3	P25OE003EC	Fundamentals of Embedded System Design (ECE)
4	P25OE004EE	Waste to Energy (EEE)
5	P25OE005ME	Industrial Safety (MED)
6	P25OE006ME	Operational Research (MED)
7	P25OE007CS	Fundamentals of Machine Learning (CSE)
8	P25OE008EC	Real Time Operating System for Embedded Applications (ECE)

Mandatory Course

S.No.	Course Code	Course Title
1	P25MC001ME	Research Methodology & IPR

List of subjects of Audit Course

S. No.	Course Code	Course Title
1	P25AD001 HS	English for Academic and Research Writing
2	P25AD002 CE	Disaster Management
3	P25AD003 HS	Sanskrit for Technical Knowledge
4	P25AD004 HS	Value Education
5	P25AD005HS	Constitution of India and Fundamental Rights
6	P25AD006 HS	Pedagogy Studies
7	P25AD007 HS	Stress Management by Yoga
8	P25AD008 HS	Personality Development through Life Enlightenment Skills

List of Laboratory Courses

S. No.	Course Code	Course Title
1	P25PC801EC	Embedded Systems Design Lab
2	P25PC802EC	Analog VLSI Design Lab
3	P25PC803EC	Real Time Operating Systems Lab
4	P25PC804EC	Digital IC Design Lab

List of Projects and Seminars

S. No.	Course Code	Course Title
1	P25PW801EC	Major Project Phase – I
2	P25PW802EC	Major Project Phase – II (Dissertation)
3	P25PC805EC	Seminar with Technical Writing

PROGRAMME CORE

Course Code	Course Title						Programme Core/ Elective
P25PC001EC	Embedded System Design						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
MPMC	3	-	-	-	40	60	3

Course Objectives

- Describe embedded systems, hardware, software components and design process of embedded system.
- Familiarize with the different IDEs for firmware development for different family of processors/controllers and discuss different tools and techniques for embedded hardware debugging.
- Understand the architecture of Cortex-M .
- Discuss the concepts of Exceptions and study the Instructions set.
- Illustrate the interfacing of real time devices like ADC, DAC and stepper motor

Course Outcomes

After completing this course, the student will be able to:

- Classify different types of embedded systems with hardware and software componentsand discuss the challenges in embedded system design.
- Summarize different tools and techniques for embedded hardware debugging.
- Explain the architecture of Cortex-M microprocessor.
- Demonstrate the skills to program Cortex-M3
- Develop programs to interface various IO devices to Cortex M3.

MODULE-I

Introduction to Embedded Systems: Embedded Systems, Classification of Embedded Systems, Embedded hardware units and devices in a system, embedded software in a system, Embedded System-on-chip, Design process in embedded system. Design Metrics and Challenges in Embedded system Design.

MODULE-II

Embedded software development process and debugging tools: Introduction, Host and target machines, Linking and locating software, Getting embedded software into target system, Issues in Hardware-Software Design and co-design, Testing, simulation and Debugging techniques and tools: Testing on Host machine, Simulators, Laboratory tools.

MODULE-III

Cortex-M Architecture: ARM instruction Set Architecture, Register Set, Processor Operating Modes, Interrupt and Processor Reset Sequence, Pipelined architecture and Data Path, Memory address Map, Bus system and Bus matrix, Memory and peripherals.

MODULE-IV

Exceptions and Instruction Set: The Cortex-M Exceptions and Interrupts, Exception and Interrupt Priority, Interrupt configuration, Handling of exceptions or interrupts.

Cortex-M Assembly Programming: Data Processing Instructions- Shift, Rotate and Logical Instructions, Basic Arithmetic Instructions, Data Movement Instructions, Bit field Instructions, Test and compare instructions, Memory access instructions, Branch and Control Instructions**.**

MODULE-V

ARM (Cortex-M3) Interfacing: GPIO Features, Interfacing of switches, LEDs, Seven Segment Display, LCD interfacing, DC Motor, Stepper Motor interfacing, I2C Interfacing

Suggested Reading:

1. Rajkamal, “Embedded Systems-Architecture, Programming and Design “, 2/10 TMH, 2012.
2. Muhammad Tahir and Kashif Javed, "ARM® Microprocessor Systems: Cortex®- M Architecture, Programming, and Interfacing", CRC Press, © 2017 by Taylor & Francis Group, LLC
3. Joseph Yiu, “The Definitive Guide to the ARM Cortex –M3”, 2/e, & Elsevier Inc., 2010.
4. Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide-Designing and Optimizing System Software”, 2006, Elsevier.
5. NPTEL-“Embedded System Design Using ARM”, https://archive.nptel.ac.in/courses/106/105/106105193/

Course Code	Course Title						Programme Core/ Elective
P25PC002EC	Analog VLSI Design						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
VLSI Design	3	-	-	-	40	60	3

Course Objectives:

- Develop a deep understanding of MOS transistor behavior, and to design and analyze single-stage amplifier topologies
- Analyze and design differential amplifier circuits and advanced current mirrors
- Evaluate the frequency response of amplifier circuits and design stable biasing and reference circuits,
- Design and analyze operational amplifiers, ensuring stability through compensation techniques.
- Understand and quantify different types of noise in analog circuits and design accurate comparators,

Course Outcomes:

- Understand and Analyze MOS Transistor Behavior and Models.
- Design and Evaluate Single Stage and Differential Amplifiers.
- Analyze Frequency Response and Reference Circuits.
- Design and Analyze Operational Amplifiers.
- Evaluate Noise Performance and Comparator Design.

MODULE- I

MOS Transistor – MOS Structure, Threshold voltage**,** Basic Electrical Properties of MOS: Ids - Vds relationships, large and small signal models of MOSFETs, body effect, Channel Length Modulation and short channel effects – velocity saturation, sub-threshold conduction, threshold voltage control, drain induced barrier lowering, gate induced drain leakage, Process Corners.

Simple CMOS current mirror, common source amplifier and Source degenerated current mirrors.

MODULE –II

Differential Amplifier: Single ended vs differential operation, basic differential pair, basic differential pair – quantitative analysis, Common mode response, Differential amplifier with MOS loads, Differential pairs with current mirror loads, large signal analysis, small signal analysis, common mode properties.

Cascode and Wilson current mirror, wide swing current mirror with enhanced output impedance.

MODULE –III

Frequency Response of Amplifiers: Miller effect, association of poles with nodes, Frequency Response: common source stage, differential pair.

Biasing and References: Establishing constant trans-conductance and band-gap reference – Positive and negative temperature coefficient basics and circuits.

MODULE – IV

Operational Amplifiers: Basic two-stage MOS Operational amplifier, characteristic parameters, design and analysis of two-stage MOS Op-Amp with given specifications. Stability and frequency compensation of Op-Amps, folded cascode OPAMP, fully differential Op-Amp and common mode feedback circuits.

MODULE –V

Noise in Amplifiers: Statistical characteristics of noise, noise spectrum, types of noise: thermal noise, flicker noise, representation of noise in circuit, Noise in common source amplifier.

Comparators: Op-Amp Based Comparators, Charge Injection Errors – Latched Comparators

Suggested Reading:

1. David Johns, Ken Martin, *Analog Integrated Circuit Design*, John Wiley & sons. 2004
2. Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, TMH.
3. *Gray*, Paul R., Hurst, Paul J., Lewis, Stephen H., Meyer, Robert G, Analysis and Design of Analog Integrated Circuits
4. Phillip E. Allen and Douglas R. Holberg "CMOS Analog Circuit Design", Oxford, 3rd edition

Course Code	Course Title						Programme Core/ Elective
P25PC003EC	Embedded Real Time Operating System						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	40	60	3

Course Objectives

- Describe the structure of Operating System.
- Distinguish between Hard and Soft Real Time Systems and analyze real time scheduling algorithms
- Illustrate the concept of Real Time Kernel and implementation of Inter Process Communication.
- Discuss the features of VxWorks and compare the commercially available RTOS's.
- Describe the features of UNIX operating system and differentiate between UNIX and POSIX.

Course Outcomes

After completing this course, the student will be able to:

- Understand the fundamental structure of Operating System.
- Compare between Hard and Soft Real time systems and analyze real time scheduling algorithms.
- Analyze the concept of Real Time Kernel and implementation of Inter Process Communication.
- Analyze the features of VxWorks and compare the commercially available RTOS's.
- Explore the features of UNIX operating system and differentiate between UNIX and POSIX.

MODULE- I

Fundamentals of Operating System: Structures of Operating System: Monolithic, Microkernel, Layered, Exo-kernel and Hybrid kernel structures, Operating System objectives and functions, Virtual Computers, Interaction of Operating system and Hardware architecture.

Evolution of operating systems: Batch, Multi programming, Multitasking, Multiuser, Parallel, Distributed and Real-Time Operating System.

MODULE- II

Real Time Operating System: Hard versus Soft Real-time systems, Jobs & Processors, Release Times, Deadlines and timing constraints, Hard and Soft timing constraints, Hard Real-time systems, Soft Real-time systems.

Real Time Scheduling Algorithms: Weighted Round Robin Approach, Priority Driven Approach, EDF scheduling Algorithm, Rate Monotonic Scheduling. Challenges in validating timing constraints in priority driven systems.

MODULE- III

Real Time Kernel: Differences between Traditional OS and RTOS, Real-time System Concepts. RTOS Kernel & Issues in Multitasking: Task Assignment, Task Priorities, Inter Task Communication & classical problems of Synchronization, Definition of Context Switching, ISRs. Critical Section. Priority inversion, Bankers Algorithm for Deadlock avoidance, Algorithm for deadlock detection. Inter Process Communication (IPC): IPC through Semaphores, Mutex, Mailboxes, Message Queues or Pipes and Event Flags.

MODULE- IV

Elementary Concepts of VxWorks: Multitasking and Task State Transition: Task Control, Task Creation and Activation, Task Stack, Task Names and IDs, Task Options, Task Information, Task Deletion and Deletion Safety, case study of traffic signal application and patient monitoring system using VxWorks Task control functions.

Memory Management: Virtual to Physical Address Mapping. Comparison of RTOS and VxWorks, μC/OS-II and RT Linux for Embedded Applications**.**

MODULE- V

Brief Review of Unix Operating Systems: UNIX Kernel: File system, Concepts of Process. Process Management: forks and execution, Programming with system calls, Process Scheduling and Shell programming.

Portable Operating System Interface (POSIX): IEEE Standard 1003.13 & POSIX real time profile. POSIX versus traditional Unix signals, overheads and timing predictability.

Suggested Reading:

1. Jane W.S. Liu,” Real Time Systems, Pearson Education”, Asia, 2001.
2. K.C. Wang, “Embedded and Real Time Operating Systems”, Springer International Publishing
3. Betcnhof, D.R., “Programming with POSIX threads”, Addison - Wesley Longman, 1997.
4. Wind River Systems, VxWorks Programmers Guide, Wind River Systems Inc.1997.
5. Jean.J. Labrosse, “MicroC/OS-II”, The CMP Books.
6. C.M. Krishna and G. Shin, Real Time Systems, McGraw-Hill Companies Inc., McGraw Hill International Editions, 1997.

Course Code	Course Title						Programme Core / Elective
P25PC004EC	Digital IC Design						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
VLSI Design	3	-	-	-	40	60	3

Course Objectives:
- Study the secondary effects of MOSFETS in DSM regime, perform timing analysis and size the inverters for optimum path delay
- Learn the Combinational Logic Design in CMOS
- Understand the sequential circuit design and the performance parameters.
- Describe the design of arithmetic building blocks
- Study the semiconductor memory design

Course Outcomes

After completing this course, the student will be able to:
- Appreciate the secondary effects of MOSFETS in DSM regime, perform timing analysis and size the inverters for optimum path delay
- Perform path optimization of CMOS gates with Logical Effort
- Compute delay and power dissipation in both dynamic and static CMOS designs, and apply pipelining techniques to optimize Sequential Circuits
- Design a simple data path for a processor and apply power reduction techniques
- Design a 6T SRAM cell and organize a memory bank

MODULE-I

Introduction to DSM CMOS Digital IC design: Quality Metrics, Trends, Design rules. CMOS Inverter – Static and Dynamic Behaviour, Performance, Power and Delay characteristics, NMOS and Pseudo-NMOS Inverters, Sizing of Inverters, Tristate Inverters. Switching Time analysis, Capacitance Calculation, Inverter Sizing for Optimal Path Delay.

MODULE-II

Designing Combinational Logic in CMOS

Static CMOS design: Complimentary CMOS, Ratioed Logic, Pass Transistor Logic, Transmission Gate Logic, and Optimizing Paths with Logical effort.

Dynamic CMOS Design: Basic Principles, Speed and Power dissipation in Dynamic Logic.

MODULE- III

Designing Sequential Circuits: Static Latches and registers, Dynamic Latches and registers, Alternative Register styles,

Non-bistable sequential Circuits. Coping with Interconnects: Capacitive, Resistive and Inductive parasitic, Advanced Interconnect Techniques.

MODULE- IV

Designing Arithmetic Building Blocks: Data paths in Digital Processor Architectures. Power and Speed Trade-offs in Data path Operators: Design- Time Power Reduction Techniques, Run-Time Power Management, Reducing the Power in Standby (or Sleep) Mode. Power Grid and Clock Design: Power Distribution Design, Clocking and Timing Issues.

MODULE- V

Semiconductor Memory Design: Introduction: Memory Organization, Types of memory, memory Timing Parameters, MOS Decoders. SRAM Cell Design: Read Write Operations, 6T SRAM Cell Layout. DRAM Cell design: 3T DRAM Cell.

Suggested Reading:

1. Jan M Rabaey, Anantha Chandrakasan and B. Nikolic, "Digital Integrated Circuits – A Design Perspective", Second Edition, PHI/ Pearson, 2003.
2. David A Hodges, Horace G Jackson and Resve A Saleh, "Analysis and Design of Digital Integrated Circuits in DSM Technology", 3rd Edition, Tata McGraw Hill, 2008
3. Wayne Wolf, Modern VLSI Design, 3rd edition, Pearson Education, 1997.
4. Neil H E Weste Kamran Eshraghian, Principles of CMOS VLSI Design a system perspective, 3rd edition, Pearson, 2005.

PROGRAMME ELECTIVE-I

Course Code	Course Title						Programme Core / Elective
P25PE001EC	Hardware Software Co-Design						Programme Elective - I
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Embedded System Design	3		-	-	40	60	3

Course Objectives:

- Describe the various Co-Design issues and Co-Synthesis algorithms.
- Discuss about the emulation techniques and its target architecture.
- Illustrate about the knowledge of firmware development process and tools.
- Apply the validation methods and adaptability.
- Apply the operation System level specification and Design

Course Outcomes:

After completing this course, the student will be able to:

- Acquire the knowledge on various co-design models
- Explore the interrelationship between Hardware and software in embedded system
- Acquire the knowledge of firmware development process and tools.
- Understand validation methods and adaptability.
- Comprehend the System level specification and Design.

MODULE- I

Co- Design Issues and Co- Synthesis Algorithms: Co- Design Models, Architectures, and Languages, A Generic Co-design Methodology. Hardware software synthesis algorithms: hardware/ software partitioning, Distributed system co-synthesis.

MODULE- II

Prototyping and Emulation: Prototyping and Emulation techniques, Prototyping and emulation environments, Future developments in emulation and prototyping architecture specialization techniques, System communication infrastructure. Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

MODULE- III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

MODULE- IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency, coordinating concurrent computations, interfacing components, Design verification, implementation verification, verification tools, interface verification.

MODULE- V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages.

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

Suggested Reading:

1. Jorgen Staunstrup, Wayne Wolf, Hardware / Software Co- Design Principles and Practice, 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, 2002, Hardware / Software Co- Design, Kluwer Academic Publishers.
3. Patrick R. Schaumont, Practical Introduction to Hardware/Software Co-design, 2010, Springer.

Course Code	Course Title						Programme Core / Elective
P25PE002EC	Quantum Computing						Programme Elective -I
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	3	-	-	-	40	60	3

Course Objectives

- Introduce fundamental quantum mechanics concepts and motivate their use in quantum computation through qubit representation
- Study multi-qubit systems, entanglement protocols, and fundamental quantum gates for computation.
- Understand quantum measurement techniques and describe composite quantum systems using density operators and entanglement measures.
- Explore the fundamentals of quantum algorithms and their advantage over classical computing approaches.
- Study quantum circuits, universal gates, quantum Fourier transform, and applications in cryptography and search algorithms.

Course Outcomes

After completing this course, the student will be able to:

- Represent qubits mathematically using computational basis, matrix form, and Bloch sphere representation.
- Analyze multi-qubit protocols like teleportation, superdense coding, and implement basic quantum logic gates.
- Compute outcomes of quantum measurements and characterize entanglement using tools like Schmidt decomposition and partial trace.
- Implement and analyze basic quantum algorithms such as Deutsch and Deutsch-Jozsa.
- Design quantum circuits for algorithms like phase estimation, order finding, and analyze their cryptographic applications.

MODULE-I

Review of Quantum Mechanics and Motivation for Quantum Computation Qubit: The qubit state - matrix and Bloch sphere representation - computational basis unitary evolution.

MODULE-II

Multi-qubit states - No-cloning theorem - Superdense coding - Pure states to Bell states – Bell inequalities. Protocols with multi-qubits: Swapping - Teleportation - gates: CNOT - Toffoli gate - NAND - FANOUT - Walsh Hadamard.

MODULE-III

Measurement: Projective operators - General, Projective and POVM measure, Ensemble: Density operators - pure and mixed ensemble - time evolution – post measurement density operator. Composite systems: Partial trace - Reduced density operator - Schmidt decomposition, Purification bipartite entanglement.

MODULE-IV

Quantum computing: Classical computing using qubits - Quantum parallelism - Deutsch's algorithm - Deutsch Josza algorithm.

MODULE-V

Quantum circuits: Basic gates - ABC decomposition - Gray codes - Universal gates - Principle of deferred and implicit measurements - Quantum Fourier transform - applications: phase estimation, order finding - factoring, discrete logarithm and hidden subgroup problems - Role of prime factoring in classical cryptography - search algorithms. Quantum error correcting codes, Physical realization of qubits.

Suggested Reading:

1. M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information, Cambridge University Press, 2010, 10th Anniversary Edition
2. Chris Bernhardt, Quantum Computing for Everyone, The MIT Press, 2019.
3. Ray LaPierre, Introduction to Quantum Computing, Springer, 2021.
4. Quantum Theory: Concepts and Methods, Asher Peres, Kluwer Academic Publishers, 1993.
5. Venkateswaran Kasirajan, Fundamentals of Quantum Computing: Theory and Practice, Springer, 2021.

<table>
<tr><th>Course Code</th><th colspan="6">Course Title</th><th>Programme Core/ Elective</th></tr>
<tr><td>P25PE003EC</td><td colspan="6">Advanced Computer Architecture</td><td>Programme Elective - I</td></tr>
<tr><td rowspan="2">Prerequisite</td><td colspan="4">Contact Hours per Week</td><td rowspan="2">CIE</td><td rowspan="2">SEE</td><td rowspan="2">Credits</td></tr>
<tr><td>L</td><td>T</td><td>D</td><td>P</td></tr>
<tr><td>Computer Organization and Architecture</td><td>3</td><td>-</td><td>-</td><td>-</td><td>40</td><td>60</td><td>3</td></tr>
</table>

Course Objectives

- Discuss fundamentals of computer design.
- Analyze quantitatively the performance parameters for different architectures.
- Explain Instruction Level Parallelism and its limitations.
- Illustrate multi-processors and thread level parallelism.
- Describe Interconnection networks.

Course Outcomes

After completing this course, the student will be able to:

- Comprehend the organization of the CPU and data path design.
- Compare the concepts of Hardwired and Micro programmed Control Unit design of generalpurpose computer.
- Understand the memory organization and hierarchy.
- Analyze I/O Interfacing concepts.
- Understand the Interconnection networks.

MODULE- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl’s law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, operations in the instruction set. Data path Design : Case studies-DMA controller

MODULE- II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory. Describe RISC architecture, memory hierarchy and issues the pipelining architecture

MODULE- III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, high performance instruction delivery- hardware based speculation. ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

MODULE- IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

MODULE- V

Inter Connection Networks: Introduction: Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.

Suggested Reading:

1. John L. Hennessy, David A. Patterson, “Computer Architecture: A Quantitative Approach”, 3rdEdition, An Imprint of Elsevier.
2. John P. Shen and Miikko H. Lipasti, “Modern Processor Design : Fundamentals of Super ScalarProcessors”, 2002, Beta Edition, McGraw Hill.
3. Kai Hwang, Faye A.Brigs., “Computer Architecture, and Parallel Processing”, McGraw Hill.
4. Dezso Sima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architecture – A Design SpaceApproach”, Pearson Education.

PROGRAMME ELECTIVE-II

Course Code	Course Title						Programme Core/ Elective
P25PE004EC	Low Power VLSI Design						Programme Elective- II
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
VLSI Design	3	-	-	-	40	60	3

Course Objectives:

- Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- Characterize and model power consumption & understand the basic analysis methods.
- Discuss leakage sources and power reduction techniques.
- Describe power estimation techniques and power minimization techniques.
- Design basic low power memory circuits.

Course Outcomes:

After completing this course, the student will be able to:

- Analyze the basic concepts of sources of power dissipation in digital IC systems and impact of power on system performance and reliability.
- Understand model power consumption and basic analysis methods.
- Explore the leakage sources and power reduction techniques.
- Analyze the different power estimation and power minimization techniques.
- Develop low power memory circuits.

MODULE- I

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of V_{dd} & V_t on speed, constraints on V_t reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

MODULE- II

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

MODULE- III

Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew V_s. Tolerable skew, chip & package co- design of clock network.

MODULE- IV

Logic Synthesis for Low Power: Power Estimation Techniques, Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

MODULE- V

Low Power Memory Design: Sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM, low power DRAM circuits, low power SRAM circuits.

Suggested Reading:

1. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000.
2. A.P. Chandrasekaran and R.W. Broadersen, "Low power digital CMOS design", Kluwer,1995
3. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
4. J.B. Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

Course Code	Course Title						Programme Core /Elective
P25PE005EC	**Semiconductor Device Modeling**						**Programme Elective- II**
Prerequisite	**Contact Hours per Week**				**CIE**	**SEE**	**Credits**
	L	**T**	**D**	**P**			
Semiconductor Physics, Linear Integrated Circuits	**3**	**-**	**-**	**-**	**40**	**60**	**3**

Course Objectives:

- Describe the characteristics and modeling of Diode.
- Discuss about the BJT model parameters and conventions.
- Illustrate about the JFET model parameters and conventions.
- Explain the levels, models and structures of the Metal Oxide Semiconductor Transistor.
- Analyze BJT, Metal Oxide Semiconductor Transistor parameter measurements.

Course Outcomes:

After completing this course, the student will be able to:

1. Understand the basics characteristics and modeling of Diode.
2. Analyze BJT model parameters and conventions.
3. Develop Comprehensive idea on JFET model parameters and conventions.
4. Understand the levels, models and structures of the Metal Oxide Semiconductor Transistor.
5. Explore the BJT, Metal Oxide Semiconductor transistor parameter measurements.

MODULE- I

PN-Junction Diode and Schottky Diode: DC Current Voltage Characteristics, Static Model, Large Signal Model, Small Signal Model, Schottky Diode and its implementation in SPICE 2, Temperature and Area effects on the Diode Model Parameter SPICE 3 Models PSPICE Models.

MODULE- II

Bipolar Junction Transistor (BJT): Transistor Conventions and Symbols, Ebers –Moll Static Model, Ebers- Moll Large Signal Model, Ebers-Moll Small Signal Model, Gummel- Poon Static Model, Gummel-Poon Large Signal Model, Gummel- Poon Small Signal Model, Temperature and Area Effects on the BJT Model Parameters, Power BJT model, SPICE 3 Models, PSPICE Models.

MODULE- III

Junction Field-Effect Transistor (JFET): Static Model, Large Signal Model and its implementation in SPICE 2, Small Signal Model and its implementation in SPICE 2, Temperature and Area Effects on the JFET Model Parameters, SPICE 3 Models, PSPICE Models.

MODULE- IV

Metal –Oxide Semiconductor Transistor (MOST): Structure and Operating Regions of the Metal Oxide Semiconductor Transistor, Level, Static Model, Level 2 Static Model, Level 1 and Level 2 Large Signal Model, Level 3 Static Model, Level 3 Large Signal Model, Effect of Series Resistances, effect of temperature on the Metal Oxide Semiconductor Transistor model parameters, SPICE 3 Models, PSPICE Model.

MODULE- V

BJT, Metal Oxide Semiconductor Transistor Parameter Measurements: Input and Model parameters, Parameter Measurements, Level 1 Model Parameters, Level 2 Model (Long-Channel) parameters, Level 2 Model (Short-Channel) parameters, Level3 Model Parameters, Measurements of capacitance, Noise, Distortion.

Suggestive Reading:

1. Giuseppe Massobrio & Paolo Antognetti, “Semiconductor Device Modeling with Spice”, second edition, Tata McGraw – Hill
2. Semiconductor Devices, Physics and Technology, Simon Sze, Ming- Kwe Lee, 3ed, ISV, WILEY Student Edition
3. Semiconductor Device Modelling, Snowden, Springer Publication

Course Code	Course Title						Programme Core/ Elective
P25PE006EC	Microchip Fabrication Techniques						Programme Elective- II
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
-	3	-	-	-	40	60	3

Course Objectives

- Introduce the semiconductor industry and provide an understanding of wafer preparation, crystal growth and clean room processes.
- Study the photolithography process and understand photoresist properties, masking and patterning steps
- Explain etching, doping and deposition techniques used in semiconductor device fabrication.
- Understand the fabrication process flow of different IC technologies and apply design rules for layouts.
- Provide knowledge about packaging processes and yield measurement in semiconductor manufacturing.

Course Outcomes

After completing this course, the student will be able to:

- Explain crystal growth techniques, wafer fabrication steps, and contamination control in semiconductor manufacturing.
- Describe and analyze the photolithography sequence, including photoresist handling, masking, and inspection methods.
- Compare dry and wet etching methods, explain doping processes (diffusion and ion implantation), and describe deposition techniques such as CVD and epitaxy.
- Outline NMOS, PMOS, CMOS, and BICMOS fabrication flows and apply design rules for stick diagrams and layouts.
- Analyze packaging requirements, yield types, and evaluate contamination effects on semiconductor yield.

MODULE-I

Overview of semiconductor industry, unit process steps for fabrication Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Contamination sources, Clean room construction; Oxidation: dry oxidation, wet oxidation.

MODULE-II

Photolithography: Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect.

MODULE-III

Etching: Dry etching, Wet etching, resist stripping; Doping: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2; Deposition: CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapor phase epitaxy, molecular beam epitaxy; Chemical mechanical polishing; Metallization.

MODULE-IV

Process flow for NMOS, PMOS, CMOS, BICMOS ICs, Novel MOS and GaN based devices. Design rules, stick diagrams and layout.

MODULE-V

Packaging: Chip characteristics, package functions, package operations

Yield Measurement: Types of Yields, Models, Effect of Contamination on Yield

Suggested Reading:

1. Peter Van Zant, Microchip Fabrication, McGraw Hill, 2014, 6th Edition.
2. S.M. Sze, VLSI Technology, McGraw-Hill, 2017, 2nd Edition (Indian).
3. Sorab K Gandhi, VLSI Fabrication Principles: Silicon and Germanium Arsenide, Wiley, 1994
4. James D Plummer, Peter B Griffin and Michael D Deal, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Pearson, 2009, 1st Edition.
5. Stephen A Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, 2001, 2nd Edition.
6. C.Y. Chang and S.M. Sze, ULSI Technology, McGraw Hill, 2000, 2nd Edition

PROGRAMME ELECTIVE-III

Course Code	Course Title						Programme Core / Elective
P25PE007EC	Machine Learning						Programme Elective- III
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Probability Theory, Linear Algebra	3	-	-	-	40	60	3

Course Objectives

- Discuss the basic theory underlying machine learning.
- To comprehend the parametric methods of learning.
- Illustrate the importance of dimensionality reduction and analyze non-parametric methods.
- To analyze various clustering methods.
- Describe the multilayer perceptron and the Back-propagation algorithm for learning the network.

Course Outcomes

After completing this course, the student will be able to:

- Understand the basic theory underlying machine learning
- To understand the parametric methods of learning
- Explore the methods of dimensionality reduction and clustering.
- Understand concept of neural networks and the learning laws.
- Evaluate the multilayer perceptron and learning rate by using the back-propagation algorithm.

MODULE- I

Introduction: Basic Definitions, Issues in Machine Learning, Applications of Machine Learning, Learning Associations, Classification, Regression, Unsupervised Learning, Reinforcement Learning, Supervised Learning, Parametric & Non-Parametric models

Data Pre-processing: Data Objects and Attribute Types, Basic Statistical Descriptions of Data, Pre-processing Missing values, Normalization, Python libraries for ML.

MODULE- II

Regression: Least squares, Single variable cost function, Multi linear regression

Logistic regression: Discriminative Classification, Hypothesis Representation, Decision Boundary, Cost function

Parameter Estimation: Bayes decision rule**,** Naive Bayes algorithm**,** Maximum Likelihood Estimation- Bernoulli Density, Gaussian Density.

MODULE- III

Unsupervised Learning-Clustering: Distance measures, Different clustering methods (Distance, Density, Hierarchical), Iterative distance-based clustering; K-Means Clustering Algorithm, Gaussian Mixed Models (GMM), Dimensionality Reduction, Eigen values, Eigen vectors, Orthogonality, Principal Component Analysis and its implementation in Python.

MODULE- IV

Supervised Learning (Regression/Classification): Introduction, Decision Tree- Entropy, Information Gain, Tree construction, ID3 – CART, Support Vector Machine, Linear learning machines and Kernel space, Making Kernels and working in feature space.

MODULE- V

Neural Networks: Perceptron, Multilayer neural network, Activation functions, Network training – Gradient Descent Optimization, Backpropagation. Evaluation metrics: SSE, RMSE, S2, Confusion matrix, Accuracy, Precision, Recall, F-score, ROC, cross-validation, hold -out. Training a Neural Network for Classification using Python.

Suggested Reading:

1. Ethem Alpaydın, Introduction to Machine Learning, Second Edition, The MIT Press.
2. Tom Michel, Machine Learning, McGraw Hill, 1997.
3. B. Yeganaranarana, Artificial Neural Networks, Prentice Hall, New Delhi, 2007.
4. Simon Haykin, Neural Networks and Learning Machines, Third Edition, Pearson Education, 2009.
5. Charu C. Aggarwal, ―Data Classification Algorithms and Applications‖, CRC Press, 2014.

E-Learning resources:

1. https://nptel.ac.in/courses/106105152
2. https://nptel.ac.in/courses/106106139

Course Code	Course Title						Programme Core / Elective
P25PE008EC	**Mixed Signal Design**						**Programme Elective- III**
Prerequisite	**Contact Hours per Week**				**CIE**	**SEE**	**Credits**
	L	**T**	**D**	**P**			
	3	**-**	**-**	**-**	**40**	**60**	**3**

Course Objectives:

- Understand and analyze the operation of switched capacitor circuits and sample-and-hold circuits.
- Study the fundamentals and performance metrics of data converters and to design and analyze various Nyquist rated A/D converter architectures.
- Explore and compare different A/D Converter architectures.
- Understand the principles of oversampling and noise shaping in sigma-delta converters.
- Analyze the operation and design of phase-locked loops

Course Outcomes:

- Analyze and design switched capacitor and sample-and-hold circuits
- Explain the fundamentals of data and different architectures of Nyquist rate D/A converters.
- Compare various Nyquist rate A/D converter architectures.
- Understand and apply oversampling concepts including delta-sigma modulation, noise shaping, and design of decimation/interpolation filters.
- Analyze the operation and performance of PLLs and DLLs

MODULE – I

Switched capacitor circuits: Basic building blocks; basic operation and analysis, inverting and non-inverting integrators, signal flow diagrams, first order filter.

Sample and hold circuits - Performance requirements, MOS sample and hold basics, clock feed through problems, S/H using transmission gates, high input impedance S/H circuits, improved S/H circuits from the point of slewing time, clock feed through cancellations.

MODULE – II

Data converter fundamentals - performance characteristics, ideal D/A and A/D converters, quantization noise. Nyquist rate D/A converters – decoder based converter, binary-scaled converters. Thermometer code converters, current mode converters, Hybrid Converters.

MODULE – III

Nyquist rate A/D Converters: Integrated converters – successive approximation converters, Cyclic A/D converters, Flash or parallel converters, two step A/D converters, pipelined A/D Converters, Time interleaved A/D Converters.

MODULE – IV

Oversampling A/D Converters: Over sampling without noise shaping and with noise shaping, First order and second order 1-bit sigma-delta modulators, system architecture, Decimating filters and interpolating filters.

MODULE – V

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

Suggested Readings:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013
4. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
5. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
6. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,

<table>
<tr><th>Course Code</th><th colspan="6">Course Title</th><th>Programme Core/ Elective</th></tr>
<tr><td>P25PE009EC</td><td colspan="6">Scripting Languages</td><td>Programme Elective- III</td></tr>
<tr><td rowspan="2">Prerequisite</td><td colspan="4">Contact Hours per Week</td><td rowspan="2">CIE</td><td rowspan="2">SEE</td><td rowspan="2">Credits</td></tr>
<tr><td>L</td><td>T</td><td>D</td><td>P</td></tr>
<tr><td>-</td><td>3</td><td>-</td><td>-</td><td>-</td><td>40</td><td>60</td><td>3</td></tr>
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Course Objectives

- Able to differentiate scripting and non-scripting languages.
- To learn Scripting languages such as PERL, TCL/TK, python and BASH
- Expertise to program in the Linux environment.
- Usage of scripting languages in IC design flow.

Course Outcomes

After completing this course, the student will be able to:

- Known about basics of Linux and Linux Networking
- Use Linux environment and write programs for automation
- Understand the concepts of Scripting languages
- Create and run scripts using PERL/TCL/Python

MODULE-I

Linux Basics: Introduction to Linux, File System of the Linux, General usage of Linux kernel & basic commands, Linux users and group, Permissions for file, directory and users, searching a file & directory, zipping and unzipping concepts.

MODULE-II:

Linux Networking: Introduction to Networking in Linux, Network basics & Tools, File Transfer Protocol in Linux, Network file system, Domain Naming Services, Dynamic hosting configuration Protocol & Network information Services.

MODULE-III

Perl Scripting: Introduction to Perl Scripting, working with simple values, Lists and Hashes, Loops and Decisions, Regular Expressions, Files and Data in Perl Scripting, References & Subroutines, Running and Debugging Perl, Modules, Object-Oriented Perl.

MODULE-IV

TCL/TK Scripting: TCL Fundamentals, String and Pattern Matching, TCL Data Structures, Control Flow Commands, Procedures and Scope, Evel, Working with Unix, Reflection and Debugging, Script Libraries, Tk Fundamentals, Tk by examples, The Pack Geometry Manager, Binding Commands to X Events, Buttons and Menus, Simple Tk Widgets, Entry and List box Widgets Focus, Grabs and Dialogs.

MODULE-V

Python Scripting: Introduction to Python, using the Python Interpreter, More Control Flow Tools, Data Structures, Modules, Input and Output, Errors and Exceptions, Classes, Brief Tour of the Standard Library.

TEXT BOOKS:

1. Practical Programming in TCL and Tk by Brent Welch, Updated for Tcl 7.4 and Tk 4.0.
2. Red Hat Enterprise Linux 4: System Administration Guide Copyright, Red Hat Inc, 2005.

Reference Books:

1. Learning Python-Mark Lutz and David Ascher, 2nd Ed. O'Reilly, 2003.
2. Learning Perl-4 Ed. Randal Schwartz, Tom Phoenix and Brain d foy. 2005.
3. Python Essentials-Samuele Pedroni and Noel Pappin. O'Reilly, 2002.
4. Programming Perl-Larry Wall, Tom Christiansen and John Orwant, 3rd Edition, O'Reilly, 2000. (ISBN 0596000278)

PROGRAMME ELECTIVE-IV

Course Code	Course Title						Programme Core / Elective
P25PE010EC	System Verilog						Programme Elective- IV
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Digital Circuits using Verilog	3	-	-	-	40	60	3

Course Objectives

- Explain the basics of System Verilog.
- Describe Combinational Logic blocks using System Verilog.
- Illustrate Sequential Logic blocks using System Verilog.
- Analyze the ability in writing test benches for verification.
- Discuss models using System Verilog.

Course Outcomes

After completing this course, the student will be able to:

- Understand the basic syntax and functions of System Verilog
- Develop the knowledge of System Verilog in building Combinational Logic Blocks
- Develop the knowledge of System Verilog in building Sequential Logic Blocks
- Analyze the functionality of the design using Test Benches
- Develop applications using the knowledge gained in System Verilog

MODULE- I

Introduction: Introduction to System Verilog, System Verilog for declaration spaces – packages, compilation- unit declarations, Simulation time units and precision, literal values & built –in data types, user defined and enumerated data types, Arrays, Structures and Unions.

MODULE- II

Combinational Logic using System Verilog Gate Models: Modules & Files, Basic Gate Models, A simple Net List, Logic Values, Continuous Assignments, Delays, Parameters, Test Benches, Multiplexers, Decoders, Priority Encoder, Adders, Parity Checkers, Test benches for combinational blocks.

MODULE- III

Sequential Logic using System Verilog Gate Models: Latches, Flip Flops, JK and T Flip Flops, Registers, Counters, Memory, Sequential multiplier, Synchronous Sequential Systems, Models of Synchronous Sequential Machines, Algorithmic state machines, Sate Machines in System Verilog.

MODULE- IV

Test Benches: Basic Test Bench, Test Bench structure, Constrained Random Simulation generation, Assertion based verification, System Verilog Simulation, System Verilog Synthesis: RTL Synthesis, Behavioral Synthesis

MODULE- V

Verification guide lines: Introduction- Verification process, plan, Methodology. A complete design modelled with System Verilog – ATM example. Behavioral modeling and transaction level modeling in System Verilog.

Suggested Reading:

1. Stuart Sutherland, Simon Davidmann and Peter Flake, System Verilog for Design, Second Edition, Springer Publications.
2. Mark Zwolinski, Digital System Design with System Verilog, Prentice Hall Publications, 2009
3. Chris Spear, System Verilog for Verification, Springer Publications

Course Code	Course Title						Programme Core / Elective
P25PE011EC	Multi Gate MOSFET Technology						Programme Elective-IV
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
VLSI Design	**3**	**-**	**-**	**-**	**40**	**60**	**3**

Course Objectives

- Understand the transition from single Gate to Multi Gate technology
- Understand the concepts of Multi Gate MOSFET's
- Familiarize with the Physics of Multi Gate MOSFET's
- Analyze the mobility in Multi Gate MOSFET's
- Design circuits using Multi Gate MOSFET's

Course Outcomes

After completing this course, the student will be able to:

- Understand the need for moving from Single Gate Technology to Multi Gate Technology
- Analyze the concepts of Multi Gate MOSFETs
- Develop knowledge of Physics in Multi Gate MOSFETs
- Develop the analytical capability on concepts of Mobility
- Develop circuits using Multi Gate MOSFET's

MODULE- I

The SOI MOSFET: MOSFET scaling, Short Channel Effects, Gate Geometry and Electrostatic integrity, Single Gate SOI MOSFET, Double Gate SOI MOSFET, Triple Gate SOI MOSFET, Surrounding Gate SOI MOSFET, Multi Gate MOSFET memory devices.

MODULE- II

Multi Gate MOSFET Technology: Introduction, Active area – Fins: Fin Width, Fin Height, Fin pinch, Fin crystal orientation, Fin surface preparation, Fin Bulk Silicon. Gate stack – patterning, threshold voltage, Gate work function requirements, Source / Drain Resistance and Capacitance, Mobility, contacts to the Fin,

MODULE- III

Physics of Multi Gate MOS system: Device electrostatics, Double Gate MOS System – Modeling assumptions, Gate Voltage effect, Semiconductor thickness effect, Asymmetry effects, Oxide thickness effect, electron tunnel current. 2-D confinement.

MODULE- IV

Mobility in Multi Gate MOSFETs: Introduction, Double Gate MOSFETs and FIN FETs – Phonon Limited Mobility, confinement of acoustic phonons, interface roughness scattering, Coulomb scattering, Temperature dependency of Mobility, High – k Dielectrics.

MODULE- V

Multi Gate MOSFET Circuit Design: Introduction**,** Digital circuit design – SRAM Design, Analog circuit design – Operational Amplifier.

Suggestive Reading:

1. FIN FETs and other Multi Gate Transistors, Springer, 2008.
2. Oleg Kononchuk and Bich- Yen Nguyen, Silicon –on – Insulator (SOI) Technology Manufacture and Applications,WP Publishing, 2014.
3. T. Yitterdal , Y. Cheng and T.A. Fjeldly, Device Modeling for Analog and RF CMOS Circuit Design, John Wiley and Sons, 2003.

Course Code	Course Title						Programme Core / Elective
P25PE012EC	VLSI Physical Design						Programme Elective – IV
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Basics of VLSI	3	-	-	-	40	60	3

Course Objectives:

- Understand the VLSI design flow, physical design steps, design rules, and different chip design methodologies.
- introduce system-level partitioning, floor planning techniques, and pin assignment strategies
- Understand the optimization methods used in cell placement, routing techniques, and clock distribution.
- Analyze performance constraints in VLSI circuits and understand timing closure using static timing analysis methods.
- Introduce physical verification techniques and DFM methodologies

Course Outcomes:

- Describe the complete VLSI design process and compare various design styles
- Apply partitioning and floor planning algorithms and perform effective pin assignment for VLSI layouts.
- Placement and routing tasks and explain clock tree synthesis and power/ground routing strategies.
- Resolve timing issues using timing-driven placement and routing techniques.
- Perform DRC, LVS, and ERC checks and apply DFM-aware routing and fixing strategies.

MODULE- I

VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multichip modules.

MODULE- II

Physical Design Optimization, Electronic Design Automation (EDA) —Netlist & System partitioning, algorithms —Introduction to Floor plan & Floor planning algorithms —Pin Assignment.

MODULE- III

Introduction to Placement, Optimization techniques, different approaches —Introduction to Routing, grid routing, global routing & their types, detailed routing & their related algorithms, power & ground routing —Basic concepts in clock networks, clock tree synthesis, clock routing.

MODULE- IV

Introduction to Timing Closure, Timing Analysis & Performance Constraints, Timing driven placement & routing — Static Timing Analysis, Topological vs logical timing analysis, False paths, Arrival time, Required arrival Time, Slacks.

MODULE- V

Physical verification - Introduction, goals and objectives, design rule check, layout versus schematic check and electrical rule check, Design for manufacturability - Introduction, DFM aware routing, DFM checks and fixing (pattern matching, MAS).

Suggested Reading:

1. Kahng, Andrew B., et al. VLSI Physical Design: from Graph partitioning to Timing closure. Springer Science & Business Media, 2011. ISBN-10: 9400790201, ISBN-13: 978-9400790209.
2. Sait, Sadiq M., and Habib Youssef. VLSI Physical Design Automation: Theory and Practice. Vol. 6. World Scientific, 1999. ISBN-10: 9788175967342, ISBN-13: 9788175967342.
3. Naveed Shervani, Algorithms for VLSI Physical Design Automation, Kluwer Academic, 1999, 3rd Edition.
4. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer, 2022, 2nd Edition

PROGRAMME ELECTIVE-V

Course Code	Course Title						Programme Core / Elective
P25PE013EC	SoC Design						Programme Elective- V
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	3	-	-	-	40	60	3

Course Objectives

- Illustrate Integration of hardware and software on a chip.
- Describe various processors.
- Design of Memory for system on chip.
- Discuss with Interconnection of various devices and reconfiguration.
- Explore various application of system on chip.

Course Outcomes

After completing this course, the student will be able to:

- Apply fundamental knowledge of digital logic design to modeling and analysis of low power in processor design.
- Understand the design concepts of processor, pipelining concepts, ARM Development Tools and Interfacing ARM with Co-processors.
- Analyze the concepts of Memory Hierarchy, Cache design and Memory Management.
- Contrast various interconnect schemes for system Development.
- Develop a simple SoC for re-configurability/low power/ASIP/NISC etc.

MODULE- I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing, System level interconnection, an approach for SOC Design, System Architecture and Complexity.

MODULE- II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

MODULE- III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

MODULE- IV

Architectural Support for System Development – ARM: The ARM Memory Interface, AMBA, ARM reference peripheral specification, Hardware system prototyping tools, The ARMUlator, JTAG Boundary scan test architecture, The ARM Debug architecture, Embedded Trace, Signal processing support.

MODULE- V

Application Studies / Case Studies: SOC Design approach, AES algorithms - Design and evaluation, Image compression – JPEG compression.

Suggested Reading:

1. Michael J. Flynn and Wayne Luk, Computer System Design System-on-Chip, Wiley India Pvt. Ltd
2. Steve Furber, ARM System on Chip Architecture, 2nd Ed., Addison Wesley Professional,2000.
3. Ricardo Reis, "Design of System on a Chip: Devices and Components, 1st Ed., Springer,2004.
4. Jason Andrews, Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology), Newnes, BK and CDROM.
5. Prakash Rashinkar, Peter Paerson and Leena Singh L, System on Chip Verification – Methodologies and Techniques, Kluwer Academic Publishers,2001.

Course Code	Course Title						Programme Core / Elective
P25PE014EC	DSP Architectures						Programme Elective- V
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Probability Theory, Linear Algebra	3	-	-	-	40	60	3

Course Objectives

- Understand fundamentals of digital signal processors and its architectures
- Remember the functional blocks and features of DSP's
- Interface the required hardware with DSP's.
- Use the DSP's in real-time applications

Course Outcomes

After completing this course, the student will be able to:

- Draw and explain fundamentals of digital signal processors and its architectures
- Remember the functional blocks and features of DSP's .
- Interface the required hardware with DSP's.
- Explore the DSP's in real-time applications.

MODULE-I

Introduction: Introduction to DSP- Evolution of DSP's-General purpose and special purpose DSP's-Fixed and floating point DSP's- selection of DSP- Basic architectures of DSP- Von neuman- Harward- modified harward architecture(VLIW) – comparison of architectures- Introduction to Commercial DSP's – Introduction to 8/16 bit DSP's.

MODULE-II

Architectures For Programmable DSP Devices: Architectures for Programmable DSP Devices: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

MODULE-III

Programmable Digital Signal Processors: Programmable Digital Signal Processors: Commercial Digital signal-processing Devices, Addressing modes of TMS320C54XX DSPs, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, interrupt programming.

MODULE-IV

Analog Devices Family Of DSP Devices: Analog Devices Family of DSP Devices: Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor.

MODULE-V

Interfacing Memory and I/O Peripherals to Programmable DSP Devices: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

Suggested Reading:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach to Digital Signal Processing - K Padmanabhan, R.Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley- IEEE Press, 2007
4. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
5. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
6. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI.

Course Code	Course Title						Programme Core / Elective
P25PE015EC	Embedded C						Programme Elective- V
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	3	-	-	-	40	60	3

Course Objectives

- Understand embedded C coding standard and basics of 8051 microcontroller
- Describe techniques of reading from and writing to port pins
- Construct structured software code with examples
- Create hardware delays to meet real-time constraints
- Develop the software architecture for intruder alarm system

Course Outcomes

After completing this course, the student will be able to:

- Explain embedded C coding standard and basics of 8051 microcontroller
- Experiment with techniques of reading from and writing to port pins
- Demonstrate structured software code with examples
- Produce hardware delays to meet real-time constraints
- Apply the software architecture for intruder alarm system.

MODULE-I

Programming Embedded Systems in C: Choice of processor and programming language Developing embedded software, Embedded C Coding Standard- Comment and White Space Rules, Module and Procedure Rules, Data Type Rules, Variable and Statement Rules

8051 Microcontroller: External interface of 8051, Reset requirements, Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption.

MODULE- II

Reading Switches: Introduction, Basic techniques for reading from port pins, Reading and writing bytes, Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Reading switch inputs (basic code), Example: Counting goats.

MODULE- III

Structured Code: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the ‘Hello Embedded World’ example, Restructuring the goat-counting example.

MODULE- IV

Meeting Real-Time Constraints

Introduction, Creating ‘hardware delays’ using Timer 0 and Timer 1, Generating 50 ms delay, Creating a portable hardware delay, The need for ‘timeout’ mechanisms, Creating loop timeouts, Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout.

MODULE- V

Case Study

Intruder Alarm System-Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions

Suggested Reading:

1. Embedded C by **Michael J. Pont** , A Pearson Education, 2007
2. Embedded C Coding Standard by Michael Barr, Barr Group, 2018
3. Programming Embedded Systems in C and C++ by Michael Barr, O’Reilly, 1999

MANDATORY COURSE

Course Code	Course Title						Mandatory Course
P25MC001ME	Research Methodology and IPR						
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	3	-	-	-	40	60	3

Course Objectives

To make students to

- Motivate to choose research as career
- Formulate the research problem, prepare the research design
- Identify various sources for literature review and data collection report writing
- Equip with good methods to analyze the collected data
- Know about IPR copyrights

Course Outcomes

At the end of this course, students will be able to**:**

- Define research problem, review and asses the quality of literature from various sources
- Improve the style and format of writing a report for technical paper/ Journal report, understand anddevelop various research designs
- Collect the data by various methods: observation, interview, questionnaires
- Analyze problem by statistical techniques: ANOVA, F-test, Chi-square
- Understand apply for patent and copyrights

MODULE - I

Research Methodology: Objectives and Motivation of Research, Types of Research, research approaches, Significance of Research, Research Methods Verses Methodology, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India, Benefits to the society in general. Defining the Research Problem: Selection of Research Problem, Necessity of Defining the Problem

MODULE - II

Literature Survey and Report writing: Importance and purpose of Literature Survey, Sources of Information, Assessment of Quality of Journals and Articles, Need of Review, Guidelines for Review, Recordof Research Review.

Report writing: Meaning of interpretation, layout of research report, Types of reports, Mechanism of writinga report.

Research Proposal Preparation: Writing a Research Proposal and Research Report, Writing Research Grant Proposal.

MODULE - III

Research Design: Meaning of Research Design, Need of Research Design, Feature of a Good Design, Important Concepts Related to Research Design, Different Research Designs, Basic Principles of ExperimentalDesign, Developing a Research Plan, Steps in sample design, types of sample designs.

MODULE - IV

Data Collection and Analysis: Methods of data collection, Data organization, Methods of data grouping, Diagrammatic representation of data, Graphic representation of data. Importance of Parametric, non- parametric test, testing of variance of two normal populations, use of Chi-square, ANOVA, F-test, z-test

MODULE - V

Intellectual Property Rights: Meaning, Nature, Classification and protection of Intellectual Property, The main forms of Intellectual Property, Concept of Patent, Patent document, Invention protection, Granting ofpatent, Rights of a patent, Licensing, Transfer of technology.

Suggested Readings:

1. C.R Kothari, Research Methodology, Methods & Technique, New Age International Publishers,2004
2. R. Ganesan, Research Methodology for Engineers‖, MJP Publishers, 2011
3. Y.P. Agarwal, Statistical Methods: Concepts, Application and Computation‖, Sterling Publications Pvt. Ltd., New Delhi, 2004
4. G.B. Reddy, Intellectual Property Rights and the Law 5th Ed. 2005 Gogia Law Agency
5. Ajit Parulekar and Sarita D'Souza, Indian Patents Law – Legal & Business Implications, MacmillanIndia Ltd, 2006

OPEN ELECTIVES

Course Code	Course Title						Core / Elective
P21OE003EC	Fundamentals of Embedded System Design						Open Elective
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
Microcontrollers	3	-	-		40	60	3

Course Objectives

- Discuss embedded system architectures, challenges and design issues.
- Describe PIC microcontroller, its features and programming.
- Illustrate ARM Microcontroller architectural details and instruction set.
- Explain ARM Memory management.
- Explore the embedded software tools to develop an embedded system.

Course Outcomes

- Understand embedded system architectures, challenges and design issues.
- Explain PIC microcontroller, its features and programming.
- Analyze ARM Microcontroller architectural details and instruction set.
- Understand ARM Memory management.
- Apply the embedded software tools to develop an embedded system.

MODULE I

Introduction to Embedded Systems: Overview of Embedded System Architecture, Challenges & Trends of Embedded Systems, Hardware Architecture, Software Architecture. Application areas of Embedded Systems & Categories of Embedded Systems. Embedded System Design & Co-Design issues and Design Cycle Process.

MODULE II

PIC 18: Family Overview, Architecture, Instruction Set, Addressing modes. Timers and Interrupts of PIC 18 and Capture/Compare and PWM modules of PIC 18.

MODULE III

ARM Architecture: ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

MODULE IV

ARM Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instruction Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions. Exception and interrupt handling.

ARM Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation Access Permissions, Context Switch.

MODULE V

Embedded Software Development Tools: Embedded Software Development Tools, Host and Target Machines, Linkers/Locators for Embedded Software, Getting Embedded Software into the Target System. Debugging Techniques.

Suggested Reading:

1. Raj Kamal, “Embedded Systems – Architecture, Programming and Design”, 2nd Edition, TMH, 2008.
2. Andrew N. Sloss, Dominic Symes, Chris Wright, “ARM Systems Developer’s Guides – Designing & Optimizing System Software”, Elsevier, 2008.
3. Mazidi, MCKinlay and Danny Causey, “PIC Microcontrollers and Embedded Systems”, Pearson Education, 2007
4. David.E.Simon, “An Embedded Software Primer,” 1st Edition, Pearson Education, 1999.
5. Jonathan W. Valvano, “Embedded Microcomputer Systems, Real Time Interfacing”, Thomas Learning, 1999.

<table>
<tr><th>Course Code</th><th colspan="6">Course Title</th><th>Core/ Elective</th></tr>
<tr><td>P25OE008EC</td><td colspan="6">Real Time Operating System for Embedded Applications</td><td>Open Elective</td></tr>
<tr><td rowspan="2">Prerequisite</td><td colspan="4">Contact Hours per Week</td><td rowspan="2">CIE</td><td rowspan="2">SEE</td><td rowspan="2">Credits</td></tr>
<tr><td>L</td><td>T</td><td>D</td><td>P</td></tr>
<tr><td>Programming in C</td><td>3</td><td>-</td><td>-</td><td>-</td><td>40</td><td>60</td><td>3</td></tr>
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Course Objectives

The course aims to

- Introduce real-time systems and their design principles, focusing on performance measures, task scheduling, fault tolerance and real-time models.
- Explain µC/OS-II RTOS concepts including multitasking, scheduling, kernel structure and inter-task communication mechanisms.
- Familiarize students with µC/OS-II RTOS functions such as task, time, semaphore, and eventand memory management, along with comparisons to other popular RTOS platforms.
- Provide in-depth knowledge of Embedded Linux, its architecture, kernel, root file system, start-up sequence and porting applications from RTOS to Linux.
- Equip students with skills in Real-Time Linux development, including kernel building, debugging, driver development, board support packages and basic C programming in Linux.

Course Outcomes

On successful completion of the course, the students will be able to:

- Analyse the architecture, performance measures, and scheduling algorithms in real-time systems.
- Implement multitasking and inter-task communication using µC/OS-II RTOS.
- Utilize µC/OS-II functions for efficient task, time, semaphore, and memory management in embedded applications.
- Configure and port applications to Embedded Linux by understanding its kernel architecture and start-up process.
- Develop and debug real-time applications on Linux, including kernel modules, embedded drivers, and board-level support.

MODULE I

REAL TIME SYSTEMS : Introduction- Issues in real time computing- Structure of a real time system- Task classes- Performance measures for real time systems- Task assignment and scheduling algorithms - Mode changes- Fault tolerant scheduling - Real Time Models.

MODULE II

µC/OS- II RTOS CONCEPTS: Foreground/Background process- Resources - Tasks - Multitasking -Priorities - Schedulers -Kernel - Exclusion - Inter task communication-Interrupts - Clock ticks - µC/OS- II Kernel structure - µC/OS- II Initialisation - Starting µC/OS- II.

MODULE III

µC/OS- II RTOS FUNCTIONS : Task Management - Time management - Semaphore management - Mutual exclusion semaphore - Event Management –Message management - Memory management - Porting µC/OS- II – Comparison and Study of Various RTOS like QNX- VX Works- PSOS.

MODULE IV

EMBEDDED LINUX : Features - Embedded Linux Distributions - Architecture of Embedded Linux - Linux Kernel Architecture – User Space -Root File System - Linux Start-Up Sequence - GNU Cross Platform Tool chain - Porting Traditional RTOS Applications to Linux.

MODULE V

REAL-TIME LINUX: Linux and Real-Time - Real-Time Programming in Linux - Hard Real-Time Linux - Building and Debugging - Building the Kernel- Integrated Development Environment - Kernel Debuggers - Embedded Drivers - Board support packages - Introduction to C linux.

Suggested Reading:

1. Krishna C.M., Kang G. Shin, "Real Time Systems", Tata McGraw-Hill Edition, 2010.
2. 2 Philip A.Laplante, "Real Time Systems Design and Analysis-An Engineers Handbook", II EditionIEEE Press, IEEE ComputerSociety Press, 2001
3. Jean J Labrosse, "MicroC/OS-II The Real Time Kernel" II Edition,CMP Books, 2002.
4. P. Raghavan,Amol Lad, SriramNeelakandan, "Embedded LinuxSystem Design and Development", Auerbach Publications, Taylor& Francis Group, 2006.
5. Christopher Hallinan, "Embedded Linux Primer, A Practical, Real-World Approach", II Edition Pearson Education, Inc., 2011.

LABORATORY COURSES

Course Code	Course Title						Core/ Programme Elective
P25PC801EC	Embedded Systems Design Lab						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	-	-	-	2	25	50	1

Course Objectives

- Describe the IDE tool for developing and executing the programs using ARM Cortex M3 (LPC 1768).
- Illustrate the usage of on-chip PWM for DC motor control.
- Explain programming with Cortex-M3/M4 to interface devices like Stepper Motor for controlling the direction.
- Illustrate the interfacing of Cortex-M3 Microcontroller with DAC, LCD, and LED to develop real time projects.
- Discuss the interface devices like Relay and Buzzer to ARM microcontroller and analyze the working of GPIO, on-chip peripherals of ARM.

Course Outcomes

After completing this course, the student will be able to:

- Demonstrate the use of IDE tool effectively for developing and executing the programs using ARM Cortex M3 (LPC 1768).
- Develop the logic to interface devices like Relay and Buzzer to ARM microcontroller and analyze the working of GPIO, on-chip peripherals of ARM
- Comprehend the usage of on-chip UART Module and interfacing display devices
- Interface devices like DC motor and stepper motor for PWM generation and to control the direction.
- Interface devices like DAC, LCD, and LED to develop real time projects.

Programming in ARM Cortex M3 (LPC 1768)

SNO	Name of the Experiment	CO Mapped
1.	Intro to IDE Tools	1
2.	Write a programs for arithmetic operations	1
3.	Interfacing LEDs and generating patterns	2
4.	Relay/buzzer/Led test	2
5.	Interfacing 7-segment display	3
6.	LCD Interfacing	3
7.	UART0 test Demonstration (To display HELLO WORLD)	3
8.	DC motor control using on chip PWM	4
9.	Stepper motor Direction control	4
10.	Program to generate Triangular, square and sinusoidal wave with DAC.	5
11.	I2C Interfacing	5

Course Code	Course Title						Programme Core/ Elective
P25PC802EC	Analog VLSI Design Lab						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
		-	-	2	25	50	1

Course Objectives:

- Observe the response of CMOS logic gates (NOT, NAND, NOR) using Cadence Virtuoso Tools.
- Analyze the response of CS Amplifiers with Current Mirrors.
- Simulate and analyze OPAMP based Circuits.
- Analyze the operation of First order sigma delta modulator.
- Assess the physical design of CMOS Inverter.

Course Outcomes

After completing this course, the student will be able to:

- Analyse the response of CMOS logic gates (NOT, NAND, NOR) using Cadence Virtuoso Tools.
- Simulate and analyse the response of CS Amplifiers with Current Mirrors.
- Analyze the responses of Differential Amplifier.
- Simulate and analyze the responses of OPAMP and its applications.
- Analyze the Physical design of CMOS Inverter.

List of Experiments

Using CAD Tools

1. Simulate and verify the MOS Operation and analyze the drain characteristics of MOS Transistors. Also observe its operating point.
2. Design and Simulation of CMOS Inverter, also analyze Transient and DC response of CMOS Inverter and compare its characteristics for different technologies.
3. Analyze the transient response of 2-input CMOS NAND and NOR gates.
4. Simulate and analyze the DC, Transient and AC response of CS Amplifier with basic current mirror.
5. Simulate and analyze the DC, Transient and AC response of CS Amplifier with cascode and Wilson current mirror.
6. Simulate and analyze the DC, Transient and AC response of Differential Amplifier with basic current mirror load.
7. Design and simulate Operational amplifier for the given specifications and analyze its DC, AC and Transient responses. Also measure Its Slew Rate.
8. Design a switched capacitor based Integrator and observe its transient and ac response.
9. Simulate and analyze the transient and ac response of CMOS Comparator.
10. Design and simulate a first order Sigma –Delta Modulator and analyze its Transient and AC Response, also analyze its Power spectrum.
11. Draw layout of CMOS Inverter and perform DRC, LVS and RC Extraction of CMOS inverter.

Course Code	Course Title						Programme Core/ Elective
P25PC803EC	Real Time Operating Systems Lab						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	-	-	-	2	25	50	1

Course Objectives

- Demonstrate Task scheduling and task management on ARM microcontroller
- Understand the concepts of IPC and demonstrate them on ARM Microcontroller
- Learn the concepts of Real time operating system (VxWorks) and its functions
- Understand the concept of file system calls and process system calls by programming in UNIX operating system

Course Outcomes

After completing this course, the student will be able to:

- Comprehend the concepts of RTOS and demonstrate them using ARM microcontroller
- Simulate the timing concepts and scheduling algorithms using Vx Works
- Simulate the Message queues and semaphore using Vx Works
- Understand the concept of file system calls and process system calls by programming in UNIX operating system

List of Experiments:

1. Write a C program to simulate the following non preemptive CPU scheduling algorithms to find "Turnaround time" &"Waiting Time" for a) FCFS b) SJF c) Round Robin d) Priority Assume all the process arrive at the same time.
2. Simulate Banker's algorithm for Deadlock avoidance.
3. Simulate Banker's algorithm for Deadlock prevention.
4. Simulate the concept of Dining Philosophers problem.
5. Demonstrate the Timing concept of Real Time applications using RTOS on ARM microcontroller kit.
6. To demonstrate the multitasking concept of RT applications using RTOS on ARM.
7. Demonstrate the SEMAPHORE concept of real time application using RTOS on ARM.
8. Demonstrate the MESSAGE QUEUES concept of real time application using RTOS on ARM.
9. Demonstrate the Mail Box concept of real time application using RTOS on ARM.
10. Demonstrate the Round Robin table scheduling using RTOS on ARM.
11. Demonstrate Priority Inversion.
12. Write the pseudo code in Linux using C/C++ to perform Print parent process ID & child process ID using Fork()

Course Code	Course Title						Programme Core/ Elective
P25PC804EC	Digital IC Design Lab						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	-	-	-	2	25	50	1

Course Objectives:

- Design combinational and sequential circuits using Verilog HDL.
- Apply simulation tool for combinational and sequential circuits RTL code and synthesize using EDA tools.
- Apply Floor plan for designed schematic of the various logic circuits using EDA tool.
- Apply placement algorithms for the various logic circuits using EDA tool.
- Apply routing algorithms for the various logic circuits using EDA tools.

Course Outcomes:

After completing this course, the student will be able to:

- Develop combinational and sequential circuits using Verilog HDL.
- Analyze the output of simulation results for combinational and sequential circuits RTL code and synthesize using EDA tools.
- Analyze Floor plan for designed schematic of the various logic circuits using EDA tool.
- Evaluate placement algorithms for the various logic circuits using EDA tool.
- Analyze routing algorithms for the various logic circuits using EDA tools.

PART-A

Design, simulation and synthesis of

1. Adder and Subtractor
2. Multiplexer and Demultiplexer
3. Encoder and Decoder
4. ROM array
5. Up/Down Counter
6. Finite State Machine

PART - B

Floor plan, Placement and Routing of

1. Adder and Subtractor
2. Multiplexer and Demultiplexer
3. Encoder and Decoder
4. ROM array
5. Up/Down Counter
6. Finite State Machine

NOTE: At least 10 experiments are to be performed.

PROJECTS AND SEMINARS

Course Code	Course Title						Programme Core/ Elective
P25PW801EC	**Major Project Phase – I**						**Core**
Prerequisite	**Contact Hours per Week**				**CIE**	**SEE**	**Credits**
	L	**T**	**D**	**P**			
	-	**-**	**-**	**24**	**100**	**-**	**12**

Course Outcomes

At the end of this course, students will be able to:

- Exposed to self-learning various topics.
- Learn to survey the literature such as books, journals and contact resource persons for the selected topic of research.
- Learn to write technical reports.
- Develop oral and written communication skills to present.
- Defend their work in front of technically qualified audience

Guidelines:

1. The abstract presentation to be made after discussing with the supervisor allotted.
2. The title of the project work will be chosen after literature review. The papers selected for literature review are to be from reputed journals only (Like IEEE, SCOPUS etc). The number of papers to be reviewed must be a minimum of 25.
3. A presentation of the abstract has to be made by the student in front of the committee (constituted by the Head of the Department) must consist of the following:
    a. Title of the project work
    b. Area of the project work
    c. List of papers reviewed in *IEEE format (minimum papers to be reviewed are 25)
    d. A review paper closest to the proposed project work may be identified.
4. Title of the project work & area of the project work cannot be modified once finalized.
5. The student must meet the supervisor allotted at least once in two weeks to appraise the progress of the project work. The supervisor will review the progress of the project work and present his/ her remarks on the progress made.
6. The report must consist of detailed problem statement, literature reviews & preliminary results in Major Project Phase –I.

Guidelines for awarding marks in CIE (Continuous Internal Evaluation): Max. Marks: 100		
Evaluation by	**Max. Marks**	**Evaluation Criteria / Parameter**
Supervisor	30	Project Status / Review(s)
	20	Report
Departmental Committee (Chairperson BOS, Head, Supervisor& Project Coordinator).	10	Relevance of the Topic
	10	PPT Preparation
	10	Presentation
	10	Question and Answers
	10	Report Preparation

Note: The Supervisor has to assess the progress of the student regularly.

Course Code	Course Title						Programme Core/ Elective
P25PW802EC	Major Project Phase – II						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	-	-	-	36	-	200	18

Course Outcomes

At the end of this course, students will be able to:

- Use different experimental techniques and will be able to use different software/ computational analytical tools
- Design and develop an experimental set up/ equipment/test rig
- Conduct tests on existing set ups/equipment and draw logical conclusions from the results after analysing them.
- Either work in a research environment or in an industrial environment
- Conversant with technical report writing and will be able to present and convince their topic of study to the engineering community.

Guidelines:

1. It is a continuation of Major Project Phase — I started in semester - III.
2. The student has to submit the report in prescribed format and also present a seminar.
3. The dissertation should be presented in standard format as provided by the department.
4. The candidate has to prepare a detailed project report consisting of introduction of the problem, problem statement, literature review, objectives of the work, methodology (experimental set up or numerical details as the case may be) of solution and results and discussion.
5. The report must bring out the conclusions of the work and future scope for the study. The work has to be presented in front of the examiners panel consisting of an approved external examiner and Chairperson BoS, & Head, Osmania University and Supervisor from the Institute.
6. The candidate has to be in regular contact with his/her Supervisor / Co- Supervisor

Guidelines for awarding marks in SEE (Semester End Examination):

Max. Marks: 200

Evaluation by	Max. Marks	Evaluation Criteria / Parameter
Supervisor	10	Regularity and Punctuality
	10	Work Progress
	30	Quality of the work which may lead to publications
	10	Analytical / Programming / Experimental Skills
	10	Report preparation in a standard format
External Examiner and Chairperson, Bos & Head (All together)	20	Power Point Presentation
	60	Quality of thesis and evaluation
	30	Innovations, application to society and Scope for
	20	Viva-Voce

Course Code	Course Title						Programme Core/ Elective
P25PC805EC	Seminar with Technical Writing						Core
Prerequisite	Contact Hours per Week				CIE	SEE	Credits
	L	T	D	P			
	-	-	-	2	50	-	1

Course Outcomes

At the end of this course, students will be able to:

- Establish motivation for any topic of interest and develop a thought process for technical presentation.
- Organize a detailed literature survey and build a document with respect to technical publications.
- Analysis and comprehension of proof-of-concept and related data.
- Effective presentation and improve soft skills.
- Make use of new and recent technology (e.g. Latex) for creating technical reports

This course is designed to develop students' ability to research, analyze, and present technical topics effectively. It emphasizes both oral communication and written documentation skills required for professional and academic settings. Students will learn to select seminar topics, conduct literature surveys, prepare technical reports, and deliver presentations. The course also covers the fundamentals of technical writing, including structure, clarity, style, citation, and ethical considerations in reporting. By the end of the course, students will be able to present complex technical concepts to diverse audiences with clarity and precision.

Guidelines for the award of marks		
SNO	**Criteria**	**Weightage of Marks**
1.	Technical Content & Depth	**15**
2.	Literature Survey & Analysis	**10**
3.	Technical Report / Writing Skills	**10**
4.	Presentation Skills (Clarity, Slides, Delivery)	**10**
5.	Question Handling & Interaction	**5**